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# Computer System Architecture MCQ 01

- RTL stands for:
- Random transfer language a.
- Register transfer language b.
- c. Arithmetic transfer language
- d. All of these
- 2. Which operations are used for addition, subtraction, increment, decrement and complement function:
- a. Bus
- b. Memory transfer
- Arithmetic operation c.
- d. All of these
- 3. Which language is termed as the symbolic depiction used for indicating the series:
- Random transfer language
- Register transfer language b.
- Arithmetic transfer language c.
- All of these d.
- 4. The method of writing symbol to indicate a provided computational process is called as a:
- Programming language a.
- Random transfer language b.
- Register transfer language c.
- d. Arithmetic transfer language
- 5. In which transfer the computer register are indicated in capital letters for depicting its function:
- Register transfer Memory transfer **b.** a.
- Bus transfer c.
- d. None of these
- 6. The register that includes the address of the memory unit is termed as the:
- MAR a.
- b. PC
- IR c.
- None of these d.
- 7. The register for the program counter is signified as
- PC MAR b. a.
- d. c.
- None of these
- 8. In register transfer the instruction register as:
- a. MAR b. PC
- IR c.
- d. None of these
- 9. In register transfer the processor register as:
- MAR a.
- b. PC
- d. RI IR C.
- 10. How many types of micro operations:
- 2 a.
- b.
- 6 c.
- d. 8

- 11. Which are the operation that a computer performs on data that put in register:
- Register transfer b. Arithmetic a.
- Logical c.
- d. All of these
- 12. Which micro operations carry information from one register to another:
- Register transfer b.
- Arithmetic
- Logical
- All of these d.
- 13. Micro operation is shown as:
- a.  $R1 \rightarrow R2$
- b. R1←R2
- Both c.
- d. None
- 14. In memory transfer location address supplied by that puts this on address bus:
  - ALU b. **CPU**
- C MAR d. **MDR**
- 15. How many types of memory transfer operation:
- 1 **b**.
- 2 c.
- 3 d. 4
- 16. Operation of memory transfer are:
- Read
- b. Write
- Both c.
- d. None
- 17. In memory read the operation puts memory address on to a register known as:
- PC
- b. **ALU**
- MAR C.
- d. All of these
- 18. Which operation puts memory address in memory address register and data in DR:
- Memory read a.
- b. **Memory write**
- Both c.
- d. None
- 19. Arithmetic operation are carried by such micro operation on stored numeric data available in
- Register a.
- b. Data
- Both c.
- d. None
- 20. In arithmetic operation numbers of register and the circuits for addition at
- ALU а.
- b. MAR
- Both
- d. None
- 21. Which operation are implemented using a binary counter or combinational circuit:
- c. Logical
- Register transfer **b.** Arithmetic
- d. All of these
- 22. Which operation is binary type, and are performed on bits string that is placed in register:
- Logical micro operation a.
- Arithmetic micro operation b.
- c. Both
- d. None

23. A micro operation every bit of a register is a: a. Constant <b>b. Variable</b>	33. In organization of a digital system register transfer of any digital system therefore it is called:
a. Constant <b>b. Variable</b> c. Both d. None	a. Digital system b. Register c. Data d. Register
24. Which operation is extremely useful in	transfer level
serial transfer of data:	34. The hinery information of course register
<ul><li>a. Logical micro operation</li><li>b. Arithmetic micro operation</li></ul>	34. The binary information of source register chosen by:
c. Shift micro operation	a. Demultiplexer <b>b. Multiplexer</b>
d. None of these	c. Both d. None
25. Which language specifies a digital system which uses specified notation:	35. Control transfer passes the function via
a. Register transfer b. Arithmetic	control_: a. Logic b. Operation
c. Logical d. All of these	c. Circuit d. All of these
26. IR stands for:	36. Register are assumed to use positive-edge-
a. Input representation	triggered:
b. Intermediate representation	a. Flip-flop b. Logics
c. Both d. None	c. Circuit d. Operation
27. HDL stands for:	37. IDE stands for:
a. Human description language	a. Input device electronics
b. Hardware description language	b. Integrated device electronic
<ul><li>c. Hardware description land</li><li>d. None of these</li></ul>	c. Both d. None
	38. ATA stands for:
28. VPCC stands for:	a. Advance technology attachment
a. Variable portable C compiler	<b>b.</b> Advance teach attachment
b. Very portable C compiler	<b>c.</b> Both d. None
c. Both	20 TEI 1 1 1 1 1 1
d. None	39. The memory bus is also referred as: <b>a.</b> Data bus  b. Address bus
29. In register transfer which system is a	c. Memory bus d. All of these
sequential logic system in which flip-flops and	c. Memory bus d. Am of these
gates are constructed:	40. How many parts of memory bus:
a. Digital system b. Register	<b>a. 2</b> b. 3
c. Data d. None	c. 5 d. 6
30. High level language C supports register	41. A three state gate defined as:
transfer technique forapplication:	a. Analog circuit b. Analog fundamentals
<b>a. Executing</b> b. Compiling	c. Both a&b <b>d. Digital circuit</b>
c. Both d. None	
21 A	42. In 3 state gate two states act as signals equal to:
31. A counter is incremented by one and memory	a. Logic 0 b. Logic 1
unit is considered as a collection of:	c. None of these <b>d.</b> Both a & b
<ul><li>a. Transfer register</li><li>b. Storage register</li><li>c. RTL</li><li>d. All of these</li></ul>	43. In 3 state gate third position termed as high
	impedance state which acts as:
32. Which is the straight forward register	a. Open circuit b. Close circuit
transfer the data from register to another register temporarily:	c. None of these d. All of above
a. Digital system	44. In every transfer, selection of register by bus is
b. Register	decided by:
c. Data	a. Control signal b. No signal
d. Register transfer operations	c. All signal d. All of above

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	45. E	Every bit o	of regi	ister has	:		
	a.	2 commo	n line	b.	3 co	mmon line	<b>;</b>
	c.	1 commo	n line	e d.	none	e of these	
	46. D	DR2 stan	ds for	:			
	<b>a.</b> ]	Double d	ata ra	te 2			
		Data doub					
		Dynamic					
	<b>d.</b> 1	Dynamic	doubl	e rate 2			
		ORAM sta					
						ess memo	ry
	b.	Synchror	<b>1ous</b>	•			access
	memo	ory	c.	Both	d.	None	
	48. W	/hich is re	eferre	d as a se	quent	ial circuit	which
						er the pro	
	a.	RTL	b.	RAM		_	
	c.	MAR	d.	All of t	hese		
	49. W	/hich ope	ration	refer bi	twise	manipulat	ion of
		nts of regi				-	
	<b>a.</b> ]	Logical n	nicro	operatio	on		
	<b>b.</b>	Arithmeti	c mic	ro opera	tion		
	c.	Shift mic	ro ope	eration			
	<b>d.</b>	None of the	hese				
	50. W	/hich sym	ıbol w	ill be us	ed to	denote an	micro
	operat						
	a.	(^)	b.	( <b>v</b> )			
	c.	Both	d.	None			
	51 w	hich sym	hol w	ill be de	note a	ın AND m	icro
	operat		001 111	٥٠ ۵٠			
		(^)	b.	(v)			
		Both	d.	None			
	52. W	/hich c	perati	on ar	e a	ssociated	with
		transfer o	-				
	a.	Logical n	nicro	operatio	n		
		Arithmeti					
		Shift mic					
		None of the	-				
	53. T	he bits are	e shift	ed and t	he fir	st flip-flop	)
						n the	
		Serial out		<b>b.</b>		al input	_
		Both	-	d.	Non		

			SCE, BL
<ul><li>56. Which shift is us</li><li>a. Logical</li><li>c. Both</li></ul>		igned binary  Arithmetic  None of the	c
57. Arithmetic left a signed number by_a. One c. Three	shift : <b>b.</b> d.	Two	
58. The variable hardware register: a. RAM c. ALU	of <b>b.</b> d.	corre RTL MAR	spond to
<ul> <li>59. In which sha signed number by the analysis.</li> <li>b. Arithmetic rights.</li> <li>c. Logical left shid. Arithmetic left shid.</li> </ul>	wo: shift s <b>ht shift</b> ft		o divide
60. Shift left is equal a. multiply by two b. add by two c. divide by two d. subtract by two	l to:		

54. How many types of shift micro operation:

4 **c.** 

55. Which shift is a shift micro operation which is used to shift a signed binary number to the left or

6

d.

b.

a.

right:

2

COMPUTER ORGANIZATION AND ARCHITECTURE BY: DK PARIDA DPT. OF CSE

- 67. Which are stages of instruction cycle:
- a. Fetch b. Decode
- c. Execute
- d. Derive effective address of the instruction
- e. All of these
- 68. Which instruction are 32 bits long, with extra 16 bits:
- a. Memory reference instruction
- **b.** Memory reference format
- **c.** Both d. None of these
- 69. Which is addressed by sign extending the 16-bit displacement to 32-bit:
- a. Memory addressb. Effectivememory address
- c. Both a and b
- d. None of these
- 70. Which are instruction in which two machine cycle are required:
- a. Instruction cycle
- b. Memory reference instruction
- c. Both d. None of these
- 71. Which instruction are used in multithreaded parallel processor architecture:
- a. Memory reference instruction
- **b.** Memory reference format
- **c.** Both d. None of these
- 72. Which instruction are arranged as per the protocols of memory reference format of the input file in a simple ASCII sequence of integers between the range 0 to 99 separated by spaces without formatted text and symbols:
- a. Memory reference instruction
- **b.** Memory reference format
- c. Both
- **d.** None of these
- 73. \_\_\_\_\_ is an external hardware event which causes the CPU to interrupt the current instruction sequence:
- a. Input interrupt b. Output interrupt
- c. Both d. None of these
- 74. ISR stand for:
- a. Interrupt save routine
- **b.** Interrupt service routine
- c. Input stages routine
- d. All of these
- 75. Which interrupt services save all the register and flags:
- a. Save interrupt
- b. Input/output interrupt
- c. Service interrupt
- d. All of these

- 76. IRET stand for:
- a. Interrupt enter
- b. Interrupt return
- c. Interrupt delete
- d. None of these
- 77. Which are benefit of input/output interrupt:
- a. It is an external analogy to exceptions
- b. The processor initiates and perform all I/O operation
- c. The data is transferred into the memory through interrupt handler
- d. All of these
- 78. Which are the not causes of the interrupt:
- a. In any single device
- b. In processor poll devices
- c. It is an external analogy to exception
- d. None of these
- 79. Which are the causes of the interrupt:
- a. In any single device
- b. In processor poll devices
- c. In a device whose ID number is stored on the address busd. All of these
- 80. Which are the functioning of I/O interrupt:
- a. The processor organizes all the I/O operation for smooth functioning
- b. After completing the I/O operation the device interrupt the processor
- c. Both d. None of these
- 81. \_\_\_\_\_with which computers perform is way beyond human capabilities:
- a. **Speed** b. Accuracy
- c. Storage d. Versatility
- 82. \_\_\_\_\_of a computer is consistently:
- a. Speed **b.** Accuracy
- e. Storage d. Versatility
- 83. GIGO stand for:
- a. Garbage-in-garbage-out
- **b.** Garbage-in garbage-occur
- **c.** Both d. None of these
- 84. How many basic operations of versatility:
- a. 5 b. 6 **c.** 4 d. 7
- 85. Which are the operation of versatility:
- a. exchange of information with the outside world via I/O device
- b. Transfer of data internally with in the central processing unit
- c. Performs of the basic arithmetic operations
- d. All of these

c.

d.

Both

None of these

c.

d.

Both

None of these

Cor	mputer System Architecture MCQ 03	9. By whom address of external function in the assembly source file supplied by when
1.	is the first step in the evolution of	activated:
	gramming languages:	a. Assembler
a.	machine language	b. Linker
b.	assembly language	c. Machine
c.	code language	d. Code
d.	none of these	
		10. Ano option is used for:
2.	Mnemonic refers to:	a. Input file
a.	Instructions	b. External file
b.	Code	c. Output file
c.	Symbolic codes	d. None of these
d.	Assembler	
		11. The assembler translates ismorphically
3.	Mnemonic represent:	mapping from mnemonic in these statements to
a.	Operation codes	machine instructions:
b.	Strings	a. 1:1
c.	Address	b. 2:1
d.	None of these	c. 3:3
		d. 4:1
4.	To represent addresses in assembly language	
we	use:	12. Assembler works inphases:
a.	String characters	a. 1
b.	Arrays	b. 3
c.	Structure	c. 2
d.	Enum	d. 4
-	Assembler works to convert assembly guage program into machine language:	13. The assembler in first pass reads the program to collect symbols defined with offsets in a
a.	Before the computer can execute it	table:
b.	After the computer can execute it	a. Hash table
c.	In between execution	b. Symbol table
d.	All of these	c. Both a& b
(		d. None of these
6.	generation computers use assembly	14 In second wass second-law anastas in
-	guage: First generation	14. In second pass, assembler creates in binary format for every instruction in program and
a. b	Third generation	then refers to the symbol table to giving every
b. <b>с.</b>	second generation	symbol anrelating the segment.
d.	fourth generation	a. Code and program
u.	Tourin goneration	b. Program and instruction
7.	Assembly language program is called:	c. Code and offset
7. a.	Object program	d. All of these
а. <b>b.</b>	Source program	G. THE OF CHESC
о. С.	Oriented program	15. which of the 2 files are created by the
d.	All of these	assembler:
		a. List and object file
8.	To invoke assembler following command are	<b>b.</b> Link and object file
give	en at command line:	c. Both a & b
a.	\$ hello.s -o hello.o	<b>d.</b> None of these
b.	\$as hello.s –o o	
c.	\$ as hello –o hello.o	16. In which code is object file is coded:
d.	\$ as hello.s –o hello.o	a. Link code
		b. Decimal code
		c. Assembly code
		d. Binary code

C.

d.

Both a & b

None of these

None of these

137			A computer having writable control
is to	issue the micro orders to:	men	nory is known as:
a.	CPU	a.	Static micro programmable
b.	Memory	b.	Dynamic micro programmable
c.	Register	c.	Both a & b
d.	Accumulator	d.	None of these
		146.	The control memory contains a set of
138	. Micro-orders generate the	wor	ds where each word is:
	ress of operand and execute instruction and		
	pare for fetching next instruction from the main	a.	Microinstruction
	mory:	b.	Program
	Physical	c.	Sets
a. L	Effective	d.	All of these
b.		a.	All of these
c.	Logical	1.45	
d.	all of above		During program execution content of
			n memory undergo changes and, but control
139	. Which of the following 2 task are	men	nory hasmicroprogram:
perf	formed to execute an instruction by MCU:		
a.	Microinstruction execution	a.	Static
b.	Microinstruction sequencing	b.	Dynamic
c.	Both a & b d. None of these	c.	Compile time
٠.	2001 to the transfer of the tr	<b>d.</b>	Fixed
140	What is the numers of misseinstruction	u.	rixeu
140	1 1	1.40	W/I + I 'C + + 1
	cutions:	148.	11 1
a.	Generate a control signal	a.	It executes "CPU" microprogram which is
b.	Generate a control signal to compile	sequ	ence of microinstructions stored in ROM
c.	Generate a control signal to execute	b.	It executes "code" microprogram which is
d.	All of these	sequ	ence of microinstructions stored in ROM
		c.	It executes "boot" microprogram which is
141	. Which microinstruction provide next	sequ	ience of microinstructions stored in ROM
inst	ruction from control memory:	d.	It executes "strap loader" microprogram
a.	Microinstruction execution	whi	ch is sequence of microinstructions stored in
b.	Microinstruction Buffer	RO	
c.	Microinstruction decoder	ROI	<b>,</b>
		140	Control memory is part of that
d.	Microinstruction Sequencing		, i <u>———</u>
1.40	XXII 1 41 C 11 1 C		addressable storage registers and used as
142	<u> </u>	tem	porary storage for data:
	roprogramed units to implement control		
proc	cess:	a.	ROM
a.	Instruction register	b.	RAM
b.	Microinstruction address generation	c.	CPU
c.	Control store microprogram memory	d.	Memory
d.	Microinstruction Buffer		·,
e.	Microinstruction decoder	150.	How many modes the address in control
			•
f.	All of these	men	nory are divided:
143	. Microcodes are stored as firmware in	a.	2
	:	b.	3
a.	Memory chips b. Registers	c.	5
c.	accumulators d. none of these	d.	7
144	. A control memory isstored in	151.	which of the following is interrupt mode:
	ne area of memory:		5
а.	Control instruction	a.	Task mode
a. b.		а. <b>b.</b>	Executive mode
	Memory instruction		
c.	Register instruction None of these	c. d.	Both a & b None of these
d.			

152. Mode of addresses in control memory are:	160. On what method search in cache memory used by the system:
a. Executive mode	memory used by the system.
b. Task mode	a. Cache directing
c. Both a & b	b. Cache mapping
d. None of these	c. Cache controlling
	d. Cache invalidation
153. Addresses in control memory is made	
byfor each register group:	process starts when a cpu with
a. Address select logic	cache refers to a memory:
<b>b.</b> Data select logic	
c. Control select logic	a. Main memory
<b>d.</b> All of these	<ul><li>b. External memory</li><li>c. Cache</li></ul>
154. There are how many register groups in	c. Cache d. All of these
control memory:	d. All of these
a. 3	162. When cache process starts hit and miss
b. <b>5</b>	rate defines in cache directory:
c. 6	
d. 8	a. during search reads
	<b>b.</b> during search writes
155. What type of circuit is used by control	<b>c.</b> during replace writes
memory to interconnect registers:	<b>d.</b> during finding writes
a. Data routing circuit	
<b>b.</b> Address routing circuit	163. In cache memory hit rate indicates:
c. Control routing circuit	a. Data from requested address is not available
<b>d.</b> None of the these	b. Data from requested address is available
156. Which memory is used to copy	<ul><li>c. Control from requested address is available</li><li>d. Address from requested address is not</li></ul>
instructions or data currently used by CPU:	available
instructions of data currently used by Cr C.	uvanaore
a. Main memory	164. In cache memory miss rate indicates:
b. Secondary memory	a. Availability of requested data
c. Cache memory	b. Availability of requested address
d. None of these	c. Non-Availability of requested data
	d. Non-Availability of requested address
157. Copy of instruction in cache memory is	
known as:	165. Which 3 areas are used by cache process:
T	a. Search, updating, invalidation
a. Execution cache	<b>b.</b> Write, updating, invalidation
<ul><li>b. Data cache</li><li>c. Instruction cache</li></ul>	<ul><li>c. Search, read, updating</li><li>d. Invalidation, updating, requesting</li></ul>
c. Instruction cache d. All of these	166. Updating writes to cache data and also to
d. All of these	· Optating writes to eache data and also to
158. Copy of data in cache memory is called:	·
a. Data cache	a. Directories
<b>b.</b> Execution cache	<b>b.</b> Memory
<b>c.</b> Address cache	c. Registers
<b>d.</b> Control cache	<b>d.</b> Folders
150	167
159. What are 2 advantages of cache memory:	167. Invalidation writes only to and
a. Reduction of average access time for CPU	erases previously residing address in memory:
memory b. Reduction of bandwidth of available memory	<ul><li>a. Folders</li><li>b. Memory</li></ul>
of CPU	c. Directory
c. Both a & b	d. Files
d. None of these	

d.

DAR

Data register

Multiplexers

c.

e. **f.**  d.

Memory of 2K,16 bits/word RAM

Accumulator register

Master clock signal

Instruction register

Control signals from bus

Internal

c.

a.

b.

d.

192.

d.

Which is the input of control unit:

Exchange

Flags

Multiplexer

Decoder

Adder

Subtractor

a.

b.

c.

d.

state as well as write back stage in CU:

Register read

a.

major state and also comes in starting of data fetch

b.

dependent on instruction and

Register write

Address

All of these

e.

f.

Computer System Architecture MCQ 04  1. Which is a type of microprocessor that is designed with limited number of instructions:	9. How many source register propagate through
a. CPU	the multiplexers:
b. RISC	1
c. ALU	
	. 1
d. MUX	a. 1
	b. <b>2</b>
2. Which unit is a pipeline system helps in	c. 3
speeding up processing over a non pipeline system:	d. 4
a. CPU	
b. RISC	
A T T T	10. How many hits of ODD salest one of the
	10. How many bits of OPR select one of the
<b>d.</b> MUX	operations in the ALU:
3. The group of binary bits assigned to perform	
a specified operation is known as:	a. 2
a. Stack register	b. 3
b. Control word	c. 4
c. Both	d. 5
d. None	
4. How many binary selection inputs in the	11. five bits of OPR select one of the operation in
control word:	<u> </u>
	the_in control register:
a. 1	
b. 7	
c. 14	a. CPU
d. 28	b. RISC
	c. ALU
5 T . 1 1.1 C 11 1	d. MUX
5. In control word three fields contain how many	
bits:	
a. 1	12. The OPR field has how many bits:
b. 2	
c. <b>3</b>	
	. 1
d. 4	a. 2
	b. 3
	c. 4
6. Three fields contains three bits each so one	d. 5
filed has how many bits in control word:	
2	
	12 To start an entertion of the start of the
b. 4	13. In stack organization the insertion operation is
c. 5	known as:
d. 6	
	a. Pop
7. How is selects the register that receives the	b. Push
information from the output bus:	c. Both
a. Decoder	d. None
<b>b.</b> Encoder	
c. MUX	
d. All of these	14. In stack organization the deletion operation is
- 1111 OI 01000	
	known as:
8. A bus organization for sevenregister:	a. Pop
a. ALU	<b>b.</b> Push
b. RISC	c. Both
c. CPU	<b>d.</b> None

d.

None

c.

d.

MUX

53.	Which addressing is an extremely influential
way	of addressing:

- a. Immediate addressing
- b. Direct addressing
- c. Register addressing
- d. Displacement addressing
- 54. Which addressing offset can be the content of

PC and also can be negative:

- a. Relative addressing
- **b.** Immediate addressing
- **c.** Direct addressing
- d. Register addressing
- 55. The length of instruction set depends on:
- a. Data size
- b. Memory size
- c. Both
- d. None
- 56. In length instruction some programs wants a complex instruction set containing more instruction, more addressing modes and greater address rang, as in case of :
- a. RISC
- b. CISC
- c. Both
- d. None
- 57. In length instruction other programs on the other hand, want a small and fixed-size instruction set that contains only a limited number of opcodes, as in case of:
- a. RISC
- b. CISC
- **c.** Both
- d. None
- 58. The instruction set can have variable-length instruction format primarily due to:
- a. Varying number of operands
- b. Varying length of opcodes in some CPU
- c. Both
- d. None
- 59. An instruction code must specify the address of the :
- a. Opecode
- b. Operand
- c. Both
- d. None

- 60. A simple\_\_\_\_\_differs widely from a Turing machine:
- a. CISC
- b. RISC
- c. CPU
- d. ALU
- 61. How many types of basically Data manipulation:
- a. 1
- b. 2
- c. 3
- d. 4
- 62. Which is data manipulation types are:
- a. Arithmetic instruction
- b. Shift instruction
- c. Logical and bit manipulation instructions
- d. All of these
- 63. Arithmetic instruction are used to perform operation on:
- a. Numerical data
- **b.** Non-numerical data
- c. Both
- d. None
- 64. How many basic arithmetic operation:
- a. 1
- b. 2
- c. 3
- d. **4**
- 65. which are arithmetic operation are:
- a. Addition
- b. Subtraction
- c. Multiplication
- d. Division
- e. All of these
- f. None of these
- 66. In which instruction are used to perform Boolean operation on non-numerical data:
- a. Logical and bit manipulation
- **b.** Shift manipulation
- c. Circular manipulation
- **d.** None of these

67.	. Which	operation is	used to s	shift the	content o	f
an	operand	to one or mo	re bits to	provide	necessar	y
vai	riation:					

- a. Logical and bit manipulation
- b. Shift manipulation
- c. Circular manipulation
- d. None of these
- 68. is just like a circular array:
- a. Data
- b. Register
- c. ALU
- d. CPU
- 69. Which control refers to the track of the address of instructions:
- a. Data control
- b. Register control
- c. Program control
- d. None of these
- 70. In program control the instruction is set for the statement in a:
- a. Parallel
- b. Sequence
- c. Both
- d. None
- 71. How many types of unconditional jumps used in program control are follows:
- a. 1
- b. 2
- c. 3
- d. 4
- 72. Which are unconditional jumps used in program control are follows:
- a. Short jump
- b. Near jump
- c. Far jump
- d. All of these
- 73. Which instruction is used in program control and used to decrement CX and conditional jump:
- a. Loop
- **b.** Shift manipulation
- **c.** Circular manipulation
- **d.** None of these

- 74. Which is always considered as short jumps:
- a. Conditional jump
- **b.** Short jump
- c. Near jump
- **d.** Far jump
- 75. Who change the address in the program counter and cause the flow of control to be altered:
- a. Shift manipulation
- b. Circular manipulation
- c. Program control instruction
- d. All of these
- 76. Which is the common program control instructions are:
- a. Branch
- b. Jump
- c. Call a subroutine
- d. Return
- e. All of these
- f. None of these
- 77. Which is a type of microprocessor that is designed with limited number of instructions:
- a. CISC
- b. RISC
- c. Both
- d. None
- 78. SMP Stands for:
- a. System multiprocessor
- b. Symmetric multiprocessor
- c. Both
- d. None
- 79. UMA stands for:
- a. Uniform memory access
- **b.** Unit memory access
- c. Both
- d. None
- 80. NUMA stands for:
- a. Number Uniform memory access
- **b.** Not Uniform memory access
- c. Non Uniform memory access
- **d.** All of these
- 81. SIMD stands for:
- a. System instruction multiple data
- b. Single instruction multiple data
- c. Symmetric instruction multiple data
- d. Scale instruction multiple data

РА-МСО	30	SCE, I
82. MIMD stands for:		
a. Multiple input multiple dat	ta 91.	Which is used to speed-up the processing:
b. Memory input multiple dat		1 1 1
c. Multiple instruction mult		
d. Memory instruction multip		Pipeline
· ·	b.	Vector processing
83. HLL stands for:	с.	Both
a. High level languages	d.	None
<b>b.</b> High level line		
<b>c.</b> High level logic	92.	Which processor is a peripheral device
<b>d.</b> High level limit	atta	ached to a computer so that the performance of a
	cor	nputer can be improved for numerical
	cor	mputations:
84. Which is a method of		
sequential process into sub opera		Attached array processor
<b>.</b>	SC <b>b.</b>	SIMD array processor
c. RISC d. Da	atabase c.	Both
	d.	None
85. How many types of array pro		
a. 1 <b>b. 2</b>		Which processor has a single instruction
c. 3 d. 4		ltiple data stream organization that manipulates
		common instruction by means of multiple
86. Which are the types of array	processor: fun	ctional units:
<ul> <li>a. Attached array processor</li> </ul>	a.	Attached array processor
b. SIMD array processor	<b>b.</b>	SIMD array processor
c. <b>Both</b> d. None	C.	Both
	d.	None

94.	Which	carry is	similar t	o rotate	without	carry
ope	rations:					

Rotate carry

#### Rotate through carry b.

c. Both

None

95. In the case of a left arithmetic shift, zeros are Shifted to the \_\_\_\_:

a.	Left	
b.	Right	
c.	Up	

Down d.

96. In the case of a right arithmetic shift the sign bit values are shifted to the\_\_\_\_:

al	takes	
nai	nce of	

Down

Right

Up

a. Left

c.

90. Parallel computing means doing sever simultaneously thus improving the perform the

87. Which are the application of vector processing:

f.

h.

88. Which types of jump keeps a 2\_byte

instruction that holds the range from- 128to127

b.

d.

89. Which types of register holds a single vector containing at least two read ports and one write

Images processing

Gene mapping

All of these

Near jump

All of these

Weather forecasting

Artificial intelligence

Experts system d.

Seismology

Aerodynamics

None of these

bytes in the memory location:

Far jump

**Short jump** 

Data system

Vector register

Data base

Memory

b.

c.

e.

g.

a.

c.

ports:

a.

b.

c.

d.

a. Data system

### b. **Computer system**

Memory c.

d. Vector register

Computer	System	Architecture	MCO	05

Computer System Architecture WCQ 03	O Have many existent of orithmetic which are		
1 A growth on great and that we as and return disite O	9. How many system of arithmetic, which are		
1. A number system that uses only two digits, 0	often used in digital system:		
and 1 is called the:	_		
a. Octal number system	a. 5		
b. Binary number system	b. 6		
c. Decimal number system	c. 3		
d. Hexadecimal number system	d. <b>4</b>		
2. In which computers, the binary number are	10. Which are the system of arithmetic, which are		
represented by a set of binary storage device such	often used in digital system:		
as flip flop:	a. Binary digit		
a. Microcomputer	b. Decimal digit		
b. Personal computer	c. Hexadecimal digit		
c. Digital computer	d. Octal digit		
d. All of these	e. All of these		
d. All of these	c. An of these		
3. A binary number can be converted into	11. In any system, there is an ordered set of		
	symbols also known as:		
Dinary number			
a. Binary number	a. Digital		
b. Octal number	b. Digit		
c. Decimal number	c. Both		
d. Hexadecimal number	d. None of these		
4 3371:1 4 : 14 6 4 6	12 371:1: 11		
4. Which system is used to refer amount of	12. Which is general has two parts in number		
things:	system:		
a. Number system	a. Integer		
<b>b.</b> Number words	b. Fraction		
<b>c.</b> Number symbols	c. Both		
<b>d.</b> All of these	d. None of these		
5 are made with some part of body,	13. MSD stand for:		
usually the hands:			
	a. Most significant digit		
a. Number words	<b>b.</b> Many significant digit		
b. Number symbols	c. Both a and b		
c. Number gestures	d. None of these		
d. All of these	Trone of these		
	14. LSD stand for:		
6are marked or written down:	a. Less significant digit		
a. Number system	b. Least significant digit		
b. Number words	c. Loss significant digit		
	d. None of these		
c. Number symbols	d. None of these		
d. Number gestures	15. The and of a number is		
7. A number symbol is called a:	defined as the number of different digits which can		
7. 11 humber symbol is cured a	occur in each position in the system:		
a. Arabic numerals	a. Base		
b. Numerals	b. Radix		
c. Both	c. Both		
d. None of these	d. None of these		
d. Profic of diese	G. MORE OF TRESC		
8. 0,1,2,3,4,5,6,7,8 and 9 numerals are called:	16. Which system has a base or radix of 10:		
a. Arabic numerals	a. Binary digit		
b. String numerals	b. Hexadecimal digit		
c. Digit numerals			
d. None of these			
u. INDIE OI HIESE	d. Octal digit		

- Nibble c.
- All of these
- 24. In which digit the value increases in power of two starting with 0 to left of the binary point and decreases to the right of the binary point starting with power -1:
- Hexadecimal a.
- b. Decimal
- **Binary** c.
- Octal

- **Subtraction** a.
- Multiply b.
- c. Divide
- All of these
- 31. Complement the subtrahend by converting all \_\_\_\_and all\_\_\_\_\_:
- 1's to 0's
- b. 0's to 1's
- Both c.
- None of these

- 32. Each device represent:
- a. 1 bit
- **b.** 2 bit
- **c.** 3 bit
- **d.** 4 bit
- 33. A 0 in the sign bit represents a and a 1 in the sign bit represents a
- a. Positive number
- b. Negative number
- c. Both
- d. None of these
- 34. How many main sign number binary codes are used:
- a. 4
- o. 5 c.
- **3** d. 6
- 35. Which are the types of binary codes number:
- a. Sign magnitude
- b. 1's complement code
- c. 2's complement code
- d. All of these
- 36. How many types of addition in the 2's complement system:
- a. 3
- b. **4**
- c. 5
- d. 6
- 37. Which are the types of addition in the 2's complement system:
- a. Both number positive
- b. A Positive number and a smaller negative number
- c. A negative number and a smaller positive number
- d. Both number negative
- e. All of these
- 38. How many important ideas to notice about these odometer readings:
- a. 1 **b. 2** c. 3 d. 4
- 39. Which are the types of important ideas to notice about these odometer readings:
- a. The MSB is the sign bit :0 for a +sign and 1 for a sign
- b. The negative number represent the 2's complement of the positive number
- c. **Both** d. All of these
- 40. Which is an algorithm or techniques used to multiply two numbers:
- a. Addition algorithm
- b. Subtraction algorithm
- c. Multiplication algorithm

- d. All of these
- 41. Which algorithm are used depending on the size of the numbers:
- a. Simple algorithm
- b. Specific algorithm
- c. Both
- d. None of these
- 42. Which algorithm is named after Volker Strassen:
- a. Strassen algorithm
- **b.** Matrix algorithm
- c. Both
- **d.** None of these
- 43. Strassen algorithm was published in
- a. 1967
- b. 1969
- c. 1987
- d. 1980
- 44. Which algorithm is used for matrix multiplication:
- a. Simple algorithm
- b. Specific algorithm
- c. Strassen algorithm
- d. Addition algorithm
- 45. Which algorithm is a divided and conquer algorithm that is asymptotically faster:
- a. Simple algorithm
- b. Specific algorithm
- c. Strassen algorithm
- d. Addition algorithm
- 46. Which method required 8 multiplication and 4 addition:
- a. Multiplication
- b. Usual multiplication
- c. Both d. None of these
- 47. Which algorithm is a multiplication algorithm which multiplies two signed binary numbers in 2's complement notation:
- Usual multiplication
- b. Booth's multiplication
- c. Both d. None of these
- 4. Which algorithm includes repeated addition of two predetermined values A and S to a product P and then performs a rightward arithmetic shift on P:
- a. Booth's algorithm
- **b.** Usual algorithm
- **c.** Multiplication algorithm
- **d.** None of these

c.

d.

**Both** 

None of these

49. Which algorithm in mathematics expresses the	
outcome of the process of division of integers by	58. In this method, the decimal number is
another:	:
a. Addition algorithm	a. Repeatedly divided by 4
b. Multiplication algorithm	b. Repeatedly divided by 2
c. Division algorithm	c. Repeatedly divided by 1
d. None of these	d. None of these
50. Which algorithm is used to find GCD of two	50 The committee of the invalidation to this area
integers:	59. The conversion of decimal fraction to binary
<ul><li>a. Multiplication algorithm</li><li>b. Division algorithm</li></ul>	fraction may be accomplished by using
<ul><li>b. Division algorithm</li><li>c. Addition algorithm</li></ul>	a. Several techniques
d. Simple algorithm	b. Simple techniques
d. Simple digorithm	c. Both d. None of these
51. Which algorithm is used as a general variant of	
a theorems, in the domain of integral numbers:	60. Which system was used extensively by early
a. Multiplication algorithm	mini computers:
b. Division algorithm	a. Decimal number <b>b.</b> Octal number
c. Addition algorithm	c. Hexadecimal number d. Binary
d. Simple algorithm	number
52. How many main approaches to algorithm for division:	61. 3 bit binary numbers can be represented by
	a. Binary number b. Decimal number
<b>a.</b> 2 b. 3 c. 4 d. 5	c. Hexadecimal number
C. 4 d. 3	d. Octal number
53. How many algorithm based on add/subtract	u. Cem number
and shift category:	62. A number system that uses eight
a. 2 b. 4	digits,0,1,2,3,4,5,6, and 7 is called an:
<b>c.</b> 3 d. 6	a. Binary number system
	b. Decimal number system
54. Which are the algorithm based on add/subtract	c. Octal number system
and shift category:	d. None of these
a. Restoring division	63. Which system each digit has a weight
b. Non-restoring division	corresponding to its position:
c. SRT division	a. Hexadecimal number system
d. All of these	b. Binary number system
	c. Decimal number system
55. Several methods for converting a	d. Octal number system
a. Decimal number to a binary number	64. Which odometer is a hypothetical device
<b>b.</b> Binary number to a decimal number	similar to the odometer of a car:
c. Octal number to a decimal number	a. Binary b. Decimal
<b>d.</b> Hexadecimal number to a binary number	c. Hexadecimal <b>d. Octal</b>
56. A popular method knows as double-dabble	65. Ancan be easily converted to its
method also knows as :	decimal equivalent by multiplying each octal digit
a. Divided-by-one method	by positional weight:
b. Divided-by-two method	a. Binary number <b>b. Octal number</b>
c. Both d. None of these	c. Hexadecimal number
	d. Decimal number
57. Which method is used to convert a large	
decimal number into its binary equivalent:	66. The simple procedure is to use:
a. Double dabble method	a. Binary-triplet method
b. Divided-by-two-method	<b>b.</b> Decimal-triplet method

c.

d.

Octal-triplet method

power of sixteen:	77. The second part of floating point designates the
<ul><li>a. Binary b. Hexadecimal</li><li>c. Octal d. None of these</li></ul>	position of the decimal point and is called:  a. Mantissa b. Binomial
c. Octal d. None of these	
68. Which number are used extensively in	c. Octal <b>d. Exponent</b>
· · · · · · · · · · · · · · · · · · ·	78. The fixed point mantissa may be
microprocessor work: a. Octal <b>b. Hexadecimal</b>	1
	a. Fraction b. Integer
c. Both d. None of these	
69. Which number is formed from a binary number	<b>c. Both</b> d. None of these
by grouping bits in groups of 4-bit each starting at	79. The number of bit required to
the binary point:	express and are determined by
a. Binary b. Octal	the accuracy desired from the computing system:
c. Decimal d. Hexadecimal	a. Exponent b. Mantissa
c. Beennai a. Hemateennai	c. Both d. None fthese
70. Which number system has a base of 16:	d. Tyone Turese
a. Binary number system	80. Which part is not physically indicated in the
b. Octal number system	register:
c. Decimal number system	a. Binary <b>b. Decimal</b>
d. Hexadecimal number system	c. Octal d. None of these
71. Counting in hex, each digit can be increment	81. The exponent contains the decimal number :
from :	a. +05 b. +03
<b>a.</b> 0 to F b. 0 to G	<b>c.</b> + <b>04</b> d. +07
c. 0 to H d. 0 to J	
	82. The first or the integer part is known
72. Which number can be converted into binary	as:
numbers by converted each hexadecimal digit to 4	a. Exponent b. Integer
bits binary equivalent using the code:	c. Binomial <b>d. None of these</b>
a. Binary number b. Decimal number	
c. Octal number d. Hexadecimal number	83. How many bits of mantissa:
	a. 4 b. 8
73. One way to convert from decimal to	<b>c. 10</b> d. 16
hexadecimal is the:	
a. Double dabble method	84. How many bit of exponent:
b. Hex dabble method	a. 4 <b>b. 6</b>
c. Binary dabble method	c. 8 d. 10
d. All of these	
	85. Which number is said to be normalized if the
74. Binary numbers can also be expressed in this	more significant position of the mantissa contains
same notation byrepresentation:	non zero digit:
a. Floating point	a. Binary point number
<b>b.</b> Binary point	b. Mantissa point number
c. Decimal point	c. Floating point number
<b>d.</b> All of these	d. None of these
75 11 6 6 4	OC William and a city of the c
75. How many parts of floating point	86. Which operation with floating point numbers
representation of a number consists:	are more complicated then arithmetic operation
a. 4 <b>b. 2</b> c. 3 d. 5	with fixed point number:
76. The first part of floating point represents a	a. Logical operation
76. The first part of floating point represents a	b. Arithmetic operation
signed fixed point number called:	c. Both d. None of these
<ul><li>a. Exponent</li><li>b. Digit</li></ul>	d. None of these
c. Number	
Number	

Mantissa

# **Computer System Architecture MCQ 06**

- 1. Which is an important data transfer technique:
- a. CPU
- b. DMA
- c. CAD
- d. None of these
- 2. Which device can be thought of as transducers which can sense physical effects and convert them into machine-tractable data:
- a. Storage devices
- b. Peripheral devices
- c. Both
- d. None
- 3. Which devices are usually designed on the complex electromechanical principle:
- a. Storage devices
- b. Peripheral devices
- c. Input devices
- d. All of these
- 4. Which disk is one of the important I/O devices and its most commonly used as permanent storage devices in any processor:
- a. Hard disk
- b. Optical disk
- c. Magneto disk
- d. Magneto Optical disk
- 5. In storage devices PC have hard disk having capacities in the range of :
- a. 12GB to 15GB
- b. 15GB to 20GB
- c. 20GB to 80GB
- d. 80GB to 85GB
- 6. Which disk is a 3.5-inch diskette with a capacity of 1.44MB:
- a. Soft disk
- b. Floppy disk
- c. Both
- d. None
- 7. Which has a large storage capacity of 2 to8GB:
- a. Magnetic tape
- b. Magnetic disk
- c. Soft disk
- d. Floppy disk

- 8. Which disk read the data by reflecting pulses of laser beams on the surface:
- a. Magnetic disk
- b. Soft disk
- c. Floppy disk
- l. Optical disk
- 9. Data access time of optical disk varies from 200 to 350minutes with transfer rate of \_\_\_\_\_
- a. 130KB/s to 400KB/s
- b. 130KB/s to 500KB/s
- c. 150KB/s to 600KB/s
- d. 150KB/s to 800KB/s
- 10. NAND type flash memory data storage devices integrated with a \_\_\_\_\_interface:
- a. ATM
- b. LAN
- c. USB
- d. DBMS
- 11. Which disk is based on the same principle as the optical disk:
- a. Optical disk
- b. Magnetic disk
- c. Magneto-optical disk
- d. All of these
- 12. WAN stands for:
- a. Wide area network
- b. Word area networkc. World area network
- d. Window area network
- 13. The human-interactive I/O devices can be further categorized as \_\_\_\_\_:
- a. Direct
- b. Indirect
- c. Both
- d. None
- 14. I/O devices are categorized in 2 parts are:
- a. Character devices
- b. Block devices
- c. Numeral devices
- d. Both a & b
- 15. UART stands for:
- a. Universal asynchronization receiver/transmitter
- b. Universal asynchronous receiver/transmitter
- c. United asynchronous receiver/transmitter
- d. Universal automatic receiver/transmitter

COMPUTER ORGANIZATION AND ARCHITECTURE BY: DK PARIDA DPT. OF CSE

\_\_\_are used for printing big charts,

drawings, maps and 3 dimensional illustrations

specially for architectural and designing purposes:

**Printers** 

**Plotters** 

Mouse

**Speakers** 

b.

c.

d.

COMPUTER ORGANIZATION AND ARCHITECTURE BY: DK PARIDA DPT. OF CSE

b.

c.

d.

a.

b.

c.

d.

Softcopy Both a & b

None of these

41. Laser printer is type of:

Non-impact printer

Impact printer

Both a & b

None of these

49. DAC stands for:	
a. Digital to analog converter	56. In devices, controller is used for:
b. Analog to digital converter	a Buffering the data
c. Only digital converter	b. Manipulate the data
d. Only analog converter	
d. Only analog converter	
50. In taxt to speech speech is expethesized using	d. Input the data
50. In text to speech, speech is synthesized using	57 Dyywhiah aignal flayy of traffic hatyyaan
lookup table ofand these clubbed together	57. By which signal flow of traffic between internal and external devices is done:
to form:	
DI 117 1	a. Only control signal
a. Phonemes, Words	b. Only timing signal
b. Phonemes, Sentences	c. Control and timing signal
c. Character, Phonemes	d. None of these
d. Word, Character	58. In devices 2 status reporting signals are:
51interface is an entity that controls data	a. BUSY
transfer from external device, main memory and or	b. READY
CPU registers:	c. Both a & b
er e registers.	d. None of these
a. I/O interface	d. Trolle of these
b. CPU interface	59. I/O module must recognize aaddress
c. Input interface	for each peripheral it controls:
d. Output interface	for each peripheral it controls.
d. Output interface	a. Long
52. The operating mode of I/O devices is	a. Long b. Same
for different device:	
for different device.	c. Unique
o Como	d. Bigger
a. Same	60. Each interaction h/w CDU and I/O madula
b. Different	60. Each interaction b/w CPU and I/O module
c. Optimum	involves:
d. Medium	D 124 42
52 T 1 11 CT/O 1 ' 41 '	a. Bus arbitration
53. To resolve problems of I/O devices there is a	b. Bus revolution
special hardware component between CPU	c. Data bus
andto supervise and synchronize all input	d. Control signals
output transfers:	
	61. Which are 4 types of commands received by
a. Software	an interface:
b. Hardware	a. Control, status, data output, data input
c. Peripheral	b. Only data input
d. None of these	c. Control, flag, data output, address arbitration
	d. Data input, data output, status bit, decoder
54. I/O modules are designed with aims to:	(A. T
a. Achieve device independence	62. Two ways in which computer buses can
b. Handle errors	communicate with memory in case of I/O devices
c. Speed up transfer of data	by using:
d. Handle deadlocks	a. Separate buses for memory and I/O device
e. Enable multi-user systems to use dedicated	b. Common bus for memory and I/O device
device	c. both a & b
f. All of these	d. none of these
55. IDE is a controller:	63. There are 2 ways in which addressing can be
controller.	done in memory and I/O device:
a. Disk	a. Isolated I/O
b. Floppy	b. Memory-mapped I/O
c. Hard	c. Both a & b
d. None of these	d. None of these

d. Buffer

71. If CPU and I/O interface share a common bus than transfer of data b/w 2 units is said to be:

**Synchronous** 

Asynchronous b.

Clock dependent c.

Decoder independent d.

b. Parallel

Both a & b c.

d. None of these

79. Modes of transfer b/w computer and I/O device are:

Programmed I/O a.

Interrupt-initiated I/O b.

c.

Dedicated processor such as IOP and DCP d.

95. \_\_\_\_interrupt method uses a register whose bits are set separately by interrupt signal for each device:

## a. Parallel priority interrupt

- b. Serial priority interrupt
- c. Both a & b
- d. None of these

96. \_\_\_\_register is used whose purpose is to control status of each interrupt request in parallel priority interrupt:

- a. Mass
- b. Mark
- c. Make
- d. Mask
- 97. The ANDed output of bits of interrupt register and mask register are set as input of:
- a. Priority decoder
- b. Priority encoder
- c. Priority decoder
- d. Multiplexer
- 98. Which 2 output bits of priority encoder are the part of vector address for each interrupt source in parallel priority interrupt:
- a. A0 and A1
- b. A0 and A2
- c. A0 and A3
- d. A1 and A2
- 99. What is the purpose
- 100. of A0 and A1 output bits of priority encoder in parallel priority:
- a. Tell data bus which device is to entertained and stored in VAD

# b. Tell subroutine which device is tentertained and stored in VAD

- c. Tell subroutine which device is to entertained and stored in SAD
- d. Tell program which device is to entertained and stored in VAD
- 101. When CPU invokes a subroutine it performs following functions:
- a. Pushes updated PC content(return address) on stack
- Loads PC with starting address of subroutine
- c. Loads PC with starting address of ALU
- d. Both a & b
- 102. DMAC stands for:

### a. Direct memory access controller

- b. Direct memory accumulator controller
- c. Direct memory access content
- d. Direct main access controller
- 103. IOP stands for:

- a. Input output processor
- 104. DCP stands for:

## a. Data communication processor

105. Which may be classified as a processor with the direct memory access capability that communicates with I/O devices:

- a. DCP
- b. IOP
- c. Both
- d. None

106. The processor that communicates with remote terminals like telephone or any other serial communication media in serial fashion is called

a. DCP

- b. IOP
- c. Both
- d. None

107. Instruction that are used for reading from memory by an IOP called\_\_\_\_\_:

- a. Commands
- b. Block diagram
- c. Interrupt
- d. None of these

108. Data communication with a remote device a special data communication is used :

- a. Multiprocessor
- b. Serial communication
- c. DCP
- d. IOP
- 109. CRC stands for:

# a. Cyclic redundancy check

Which is used for synchronous data, PID is process ID, followed by message, CRC code and EOP indicating end of block:

- a. DCP
- b. CRC
- c. IOP
- d. SYNC
- 111. Which is commonly used in high –speed devices to realize full efficiency of communication link:
- a. Transmission

### b. Synchronous communication

- c. Multiprocessor
- d. All of these

b.

c.

d.

Shared memory multiprocessor

None of these

Distributed memory multiprocessor

on med	5 (L), 9D
112. Multiprocessor use than two	120. The memory capacity in system is
CPUs assembled in single system unit:	considered because the connecting processors are
a. One or More	used :
b. Two or More	
c. One or One	a. Network
d. Two or Two	b. Internet
	c. Intranet
113. Which refers the execution of various	d. None of these
software process concurrently:	d. Trone of these
a. Multiprocessor	121. Intercrosses arbitration system for
b. Serial communication	multiprocessor shares a:
c. DCP	mareprocessor shares a
d. IOP	a. Primary bus
u. 101	b. Common bus
114. Which is used for this and known as high	c. Domain bus
speed buffer exist with almost each process?	d. All of these
speed burier exist with armost each process:	d. All of these
a. Primary	122. Which is used to decentralize the
b. RAM	decision to avail greater flexibility to the system
c. Cache	that makes processor or microprocessor in a very
d. None of these	short:
	5.101.0
115. Data and instructions are accessed from	a. Arbitration
local memory and global memory that is used	b. Centralized
by:	c. Both a & b
a. Internetworking facilities	d. None of these
b. Interconnection facilities	d. Trone of these
c. Both a & b	123. Which is signal tells that an arbitration of
d. None of these	the access bus is possible during interprocessing:
116. Multiprocessor uses large caches but	and access cas is possion during interprocessing.
limited process that shares	a. DBA
a. Memory bus	b. BAP
b. Single memory bus	c. BNA
c. Double memory bus	d. None of these
d. None of these	d. Trone of these
117. Distributed are shares also referred to as	124. Which signal bus request:
tightly coupled and loosely coupled multiprocessor	12 ii winen signar sus request.
respectively and hence called	a. BAP
a. Coupled multiprocessor	b. BNA
b. Shared multiprocessor	c. BAL
c. Distributed multiprocessor	d. DBA
d. None of these	u. DDA
118. Which consist if a numbers of processor	125. Which signal on the bus indicates that
can be accessed among various shared memory	request from process arbitration is to be processed:
modules?	request from process aroundfrom is to be processed.
	a. BAL
<ul><li>a. Coupled memory multiprocessor</li><li>b. Shared memory multiprocessor</li></ul>	a. BAL b. BREQ
c. Distributed memory multiprocessor	c. BM4
d. None of these	d. DBA
119. Which keeps a number of processors in	u. DDA
which virtual storage space is assigned for	126. Which signal is exchange information by
redundant execution:	
	bus: a. BECH
a. Coupled memory multiprocessor	a. BECH

b.

c.

d.

BM4 BAL

- 127. Which signal on bus applies +1 to the priority of resolution circuits of the arbitration designate a new arbitration:
- a. BM4
- b. BAL
- c. BNA
- d. DBA
- 128. Which signal create 3 lines of bus in which signals from the encoded number of processors:
- a. BM1 to BM3
- b. BAL
- c. Both
- d. None of these
- 129. Which signal request the validation signal make active if its logic level is 0 and validate signals from BM1 to BM3:
- a. BAL
- **b. BM4**
- c. BNA
- d. All of these
- 130. Which signal represents synchronization signal decided by interprocess arbitration with a certain delay or signal DMA:
- a. BAL
- b. BNA
- c. Both
- d. None of these
- 131. In which condition only one process holds a resource at a given time:
- a. Mutual exclusion
- b. Hold and wait
- c. Both
- d. None of these
- 132. In which condition one process holds the allocated resources and other waits for it:
- a. No preemption
- b. Hold and wait
- c. Mutual exclusion
- d. All of these
- 133. In which condition resource is not removed from a process holding:
- a. Synchronization problem
- b. No preemption
- c. Hold and wait
- d. None of these

- 134. In which condition busy waiting, programmer error, deadlock or circular wait occurs in interprocessing:
- a. Synchronization problem
- b. No preemption
- c. Hold and wait
- d. None of these
- 135. Mechanism can be referred to as adding a new facility to the system hence known as

\_\_\_\_:

- a. Process
- b. Arbitration
- c. Both a & b
- d. None of these
- 136. Which is a mechanism used by the OS to ensure a systematic sharing of resources amongst concurrent resources:
- a. Process synchronous
- b. Process system
- c. Process synchronization
- d. All of these
- 137. \_\_\_\_\_ is basically sequence of instructions with a clear indication of beginning and end for updating shared variables
- a. Critical section
- b. Entry section
- c. Remainder section
- d. All of these
- 138. Which provides a direct hardware support to mutual exclusion
- a. Test-and-set(TS)
- b. Swap instruction
- c. Wait instruction
- d. Signal instruction
- 139. A process waiting to enter its critical section may have to wait for unduly\_\_\_\_:
- a. Short time or may have to wait forever
- b. Long time or may have to wait forever
- c. Short time or may have to wait for long time
- d. Long time or may have to wait for short time
- 140. Which is a modified version of the TS instruction which is designed to remove busy-waiting:
- a. Swap instruction
- b. Wait instruction
- c. Signal instruction
- d. Both b & c

141.	PCB stands for:	150	. The exclusion between processes is
a.	Process control block	ensu	ared by a third semaphore called:
		a.	Mutex
142.	gets activated whenever the process	b.	Mutual
enco	ounters a busy condition code:	c.	Memory
a.	Wait instruction	d.	All of these
b.	Signal instruction		
c.	Both a & b	151	semaphore provides mutual
d.	None of these	excl	usion for accesses to the buffer pool and is
			alized to the value:
143.	are new and mutually exclusive		
opei	ration:	a.	Mutex
a.	Wait instruction	b.	Mutual
b.	Signal instruction	c.	Memory
c.	Both a & b	d.	All of these
d.	None of these		
		152	. Which processes access and manipulate
144.	gets activated whenever a		shared data concurrently:
	cess leaves the critical region and the flag is set		· · · <b>y</b> ·
to fa		a.	Micro processes
a.	Wait instruction	b.	Several processes
b.	Signal instruction	c.	Both
c.	Both a & b	d.	None of these
d.	None of these	u.	Trone of these
u.	Trone of these	153	. Which section is basically a sequence of
145.	. Which represent an abstraction of many		ruction with a clear indication of beginning and
	ortant ideas in mutual exclusion:		for updating shared variables:
a.	Process synchronous	Cild	for updating shared variables.
b.	Process system	a.	Racing section
c.	Semaphores	а. <b>b.</b>	Critical section
d.	All of these	о. С.	Both
u.	This of these	d.	None of these
146.	. A semaphore is ainteger	u.	None of these
	able upon which two atomic operations wait	154	. In which section only one process is
	signal are defined:		wed to access the shared variable and all other
	Negative integer		
a. <b>b.</b>	Non- Negative integer	nave	e to wait:
	Positive integer		Critical section
c. d.	None of these	<b>a.</b> b.	
u.	None of these		Racing section
147	Which are anotion is averaged as soon as	C.	Entry section
147.	1	d.	Remainder section
proc	eess exits from a critical section:	155	XXII 1 11 6 11 1
	Wait	155	±
a.	Wait	sect	ion:
b.	Signal		M. 1 1 1
c.	Both a & b	a.	Mutual exclusion
d.	None of these	b.	Progress
		c.	Bounded wait
148.		d.	All of these
a.	Conditional critical region		
		156	E
149.	<u></u>		a process that is executed when the process
leve	l programming language:	inte	nds to enter its critical section:
a.	CPU	a.	Critical section
b.	ALU	b.	Entry section
c.	DDR	c.	Reminder section
d.	CCR	d.	None of these

- 157. Which section refer to the code segment where a shared resource is accessed by the process:
- a. Reminder section
- b. Entry section
- c. Both
- d. None of these
- 158. Which section is the remaining part of a process's code:
- a. Racing section
- b. Critical section
- c. Entry section
- d. Reminder section
- 159. How many conditions for controlling access to critical section:
- a. 2
- b. 4
- c. 3
- d. 5
- 160. Which instruction provides a direct hardware support to mutual exclusion:
- a. SP instruction
- b. TS instruction
- c. Both
- d. None of these
- 161. Which instruction also improves the efficiency of the system:
- a. Swap instruction
- b. TS instruction
- c. Both
- d. None of these
- 162. Which instruction allows only one concurrent process to enter the critical section:
- a. RP instruction
- b. SP instruction
- c. TS instruction
- d. None of these
- 163. Which section problem can be solved simply in a uniprocessor environment if the we are able to prevent the occurrence of interrupt during the modification of a shared variable:
- a. Entry section
- b. Critical section
- c. Non-critical section
- d. None of these

- 164. The problem of readers and writers was first formulated by \_\_\_\_\_:
- a. P.J. Courtois
- b. F.Heymans
- c. D.L. Parnas
- d. All of these
- 165. Which is a situation in which some process wait for each other's actions indefinitely:
- a. Operating system
- b. Deadlock
- c. Mutex
- d. None of these
- 166. \_\_\_\_\_system handles only deadlocks caused by sharing of resources in the system:
- a. Operating system
- b. Deadlock
- c. Mutex
- d. None of these
- 167. A deadlocks occurs when the how many conditions are met:
- a. 1
- b. 2
- c. 3
- d. 4
- 168. Which are the characteristics of deadlocks:
- a. Mutual exclusion
- b. Hold and wait
- c. No pre-emption
- d. Circular wait
- e. All of these
- 169. RAG stands for:
- a. Resource allocation graph
- 170. How many events concerning RAG can occur in a system:
- ı. 1
- b. 2
- c. 3
- d. 4
- 171. Which are the events concerning RAG can occur in a system:
- a. Request for a resource
- b. Allocation of a resource
- c. Release of resource
- d. All of these

172. How many methods for handling	181. The various file operation are:
deadlocks:	a. Crating a file b. Writing a file
a. 1 b. 2	c. Reading a file
c. 3 d. 4	d. Repositioning within a file
c. 3 u. 4	
	e. Deleting a file truncating a file
173. Which are the method for handling	f. All of these
deadlocks:	
	182. Which operations are to be performed on
a. Deadlock prevention	a directory are:
b. Deadlock avoidance	a. Search for a file b. Create a file
	c. Delete a file d. List a directory
d. All of these	e. Rename a file
	f. Traverse the file system
174. How many condition that should be met	g. All of these
in order to produce a deadlock:	
1	183. Which memory is assembled between
a. 2 b. <b>4</b>	main memory and CPU:
	•
c. 6 d. 8	a. Primary memory b. Cache memory
	c. Both a & b d. None of these
175. Which are the condition that should be	
met in order to produce a deadlock:	184. Which is considered as semi-conductor
•	memory, which is made up of static RAM:
a. Mutual exclusion b. Hold and Wait	a. Primary memory b. <b>Cache memory</b>
	c. Both a & b d. None of these
	c. Both a & b d. None of these
<b>d.</b> Circular wait e. <b>All of these</b>	
	185. Which is one of the important I/O
176. In protocol each process can make a	devices and is most commonly used as permanent
request only in an:	storage device in any processor:
1 ,	a. Soft disk b. <b>Hard disk</b>
a. <b>Increasing order</b> b. Decreasing order	c. Both a & b d. None of these
	c. Both a & b d. None of these
c. Both a & b d. None of these	106
	can read any printed character by
177. In protocol above mentioned	comparing the pattern that is stored in the
protocol are used then the circular wait-	computer:
condition can not hold:	a. SP b. CCR
	c. RAG d. <b>OCR</b>
a. 1 b. <b>2</b>	
	187. Which system is a typical example of the
c. 3 d. 4	
	readers and writers problem:
178. Which state refers to a state that is not	a. Airline reservation system
safe not necessarily a deadlocked state:	b. Airport reservation system
	c. Both
a. Safe state b. <b>Unsafe state</b>	d. None of these
5 1 0 1 1 N 0 1	188. Which lock can arise when two
c. Both a & b d. None of these	
170	processes wait for phone calls from one another:
179 a direct arrow is drawn from	
the process to the resource rectangle to represent	a. Spine lock b. <b>Dead lock</b>
each pending resource request:	c. Both d. None of these
a. TS b. SP	
c. CCR d. RAG	189. Which lock is more serious than
	indefinite postponement or starvation because it
180 The attributes of a file area	
180. The attributes of a file are: affect more than one job:	
a. Name b. Identifier	
c. Types d. Location	a. <b>Deadlock</b> b. Spinelock
e. Size f. Protection	c. Both d. None of these
g. Time, date and user identification	
h. All of these	