SRINIX COLLEGE OF ENGINEERING,BALASORE

PROBABLE QUESTIONS AND ANSWERS

3rd SEMESTER

SUBJECT-DLD BRANCH-CSE

1. Any signed negative binary number is recognised by its _____
a) MSB
b) LSB
c) Byte
d) Nibble
View Answer
Answer: a
Explanation: Any negative number is recognized by its MSB (Most Significant Bit).
If it's 1, then ít's negative, else if it's 0, then positive.

2. The parameter through which 16 distinct values can be represented is known as _____
a) Bit
b) Byte
c) Word
d) Nibble
View Answer
Answer: c
Explanation: It can be represented up to 16 different values with the help of a Word. Nibble is a combination of four bits and Byte is a combination of 8 bits. It is "word" that is said to be a collection of 16-bits on most of the systems.

3. If the decimal number is a fraction then its binary equivalent is obtained by _____ the number continuously by 2.
a) Dividing
b) Multiplying
c) Adding
d) Subtracting
View Answer
Answer: b
Explanation: On multiplying the decimal number continuously by 2, the binary equivalent is obtained by the collection of the integer part. However, if it's an integer, then it's binary equivalent is determined by dividing the number by 2 and collecting the remainders.

4. The representation of octal number (532.2)8 in decimal is _____
a) (346.25)10
b) (532.864)10
c) (340.67)10
d) (531.668)10
View Answer
Answer: a
Explanation: Octal to Decimal conversion is obtained by multiplying 8 to the power of base index along with the value at that index position.
$(532.2)8 = 5 * 8^2 + 3 * 8^1 + 2 * 8^0 + 2 * 8^{-1} = (346.25)10$

5. The decimal equivalent of the binary number (1011.011)2 is _____
a) (11.375)10
b) (10.123)10
c) (11.175)10
d) (9.23)10
View Answer
Answer: a
Explanation: Binary to Decimal conversion is obtained by multiplying 2 to the power of base index along with the value at that index position.

$1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1*2^0 + 0 * 2^{-1} + 1 * 2^{-2} + 1 * 2^{-3} = (11.375)10$
Hence, $(1011.011)2 = (11.375)10$

6. An important drawback of binary system is _____
a) It requires very large string of 1's and 0's to represent a decimal number
b) It requires sparingly small string of 1's and 0's to represent a decimal number
c) It requires large string of 1's and small string of 0's to represent a decimal number
d) It requires small string of 1's and large string of 0's to represent a decimal number
View Answer
Answer: a
Explanation: The most vital drawback of binary system is that it requires very large string of 1's and 0's to represent a decimal number. Hence, Hexadecimal systems are used by processors for calculation purposes as it compresses the long binary strings into small parts.

7. The decimal equivalent of the octal number $(645)_8$ is _____
a) $(450)_{10}$
b) $(451)_{10}$
c) $(421)_{10}$
d) $(501)_{10}$
View Answer
Answer: c
Explanation: Octal to Decimal conversion is obtained by multiplying 8 to the power of base index along with the value at that index position.
The decimal equivalent of the octal number $(645)_8$ is $6 * 8^2 + 4 * 8^1 + 5 * 8^0 = 6 * 64 + 4 * 8 + 5 = 384 + 32 + 5 = (421)_{10}$.

8. The largest two digit hexadecimal number is _____
a) (FE)16
b) (FD)16
c) (FF)16
d) (EF)16
View Answer
Answer: c
Explanation: (FE)16 is 254 in decimal system, while (FD)16 is 253. (EF)16 is 239 in decimal system. And, (FF)16 is 255. Thus, The largest two-digit hexadecimal number is (FF)16.

9. Representation of hexadecimal number (6DE)H in decimal:
a) $6 * 16^2 + 13 * 16^1 + 14 * 16^0$
b) $6 * 16^2 + 12 * 16^1 + 13 * 16^0$
c) $6 * 16^2 + 11 * 16^1 + 14 * 16^0$
d) $6 * 16^2 + 14 * 16^1 + 15 * 16^0$
View Answer
Answer: a
Explanation: Hexadecimal to Decimal conversion is obtained by multiplying 16 to the power of base index along with the value at that index position.
In hexadecimal number D & E represents 13 & 14 respectively.
So, $6DE = 6 * 16^2 + 13 * 16^1 + 14 * 16^0$.

10. The quantity of double word is _____
a) 16 bits
b) 32 bits
c) 4 bits
d) 8 bits
View Answer
Answer: b

11. The given hexadecimal number (1E.53)16 is equivalent to _____
a) (35.684)8
b) (36.246)8
c) (34.340)8
d) (35.599)8
View Answer
Answer: b
Explanation: First, the hexadecimal number is converted to it's equivalent binary form, by writing the binary equivalent of each digit in form of 4 bits. Then, the binary equivalent bits are grouped in terms of 3 bits and then for each of the 3-bits, the respective digit is written. Thus, the octal equivalent is obtained.
(1E.53)16 = (0001 1110.0101 0011)2

= (00011110.01010011)2
= (011110.010100110)2
= (011 110.010 100 110)2
= (36.246)8.

12. The octal number (651.124)8 is equivalent to _____
a) (1A9.2A)16
b) (1B0.10)16
c) (1A8.A3)16
d) (1B0.B0)16
View Answer
Answer: a
Explanation: First, the octal number is converted to it's equivalent binary form, by writing the binary equivalent of each digit in form of 3 bits. Then, the binary equivalent bits are grouped in terms of 4 bits and then for each of the 4-bits, the respective digit is written. Thus, the hexadecimal equivalent is obtained.
(651.124)8 = (110 101 001.001 010 100)2
= (110101001.001010100)2
= (0001 1010 1001.0010 1010)2
= (1A9.2A)16.

13. The octal equivalent of the decimal number (417)10 is _____
a) (641)8
b) (619)8
c) (640)8
d) (598)8
View Answer
Answer: a
Explanation: Octal equivalent of decimal number is obtained by dividing the number by 8 and collecting the remainders in reverse order.
8 | 417
8 | 52 — 1
8 | 6 – 4
So, (417)10 = (641)8.

14. Convert the hexadecimal number (1E2)16 to decimal.
a) 480
b) 483
c) 482
d) 484
View Answer
Answer: c
Explanation: Hexadecimal to Decimal conversion is obtained by multiplying 16 to the power of base index along with the value at that index position.
(1E2)16 = $1 * 16^2 + 14 * 16^1 + 2 * 16^0$ (Since, E = 14)
= 256 + 224 + 2 = (482)10.

15. (170)10 is equivalent to _____
a) (FD)16
b) (DF)16
c) (AA)16
d) (AF)16
View Answer
Answer: c
Explanation: Hexadecimal equivalent of decimal number is obtained by dividing the number by 16 and collecting the remainders in reverse order.
16 | 170
16 | 10 – 10
Hence, (170)10 = (AA)16.

16. Convert (214)8 into decimal.
a) (140)10
b) (141)10
c) (142)10
d) (130)10
View Answer
Answer: a
Explanation: Octal to Decimal conversion is obtained by multiplying 8 to the power of base index along with the

value at that index position.
$(214)8 = 2 * 8v + 1 * 8^1 + 4 * 8^0$
$= 128 + 8 + 4 = (140)10.$

17. Convert (0.345)10 into an octal number.
a) (0.16050)8
b) (0.26050)8
c) (0.19450)8
d) (0.24040)8
View Answer
Answer: b
Explanation: Converting decimal fraction into octal number is achieved by multiplying the fraction part by 8 everytime and collecting the integer part of the result, unless the result is 1.
0.345*8 = 2.76 2
0.760*8 = 6.08 6
00.08*8 = 0.64 0
0.640*8 = 5.12 5
0.120*8 = 0.96 0
So, (0.345)10 = (0.26050)8.

18. Convert the binary number (01011.1011)2 into decimal.
a) (11.6875)10
b) (11.5874)10
c) (10.9876)10
d) (10.7893)10
View Answer
Answer: a
Explanation: Binary to Decimal conversion is obtained by multiplying 2 to the power of base index along with the value at that index position.
$(01011)2 = 0 * 2^4 + 1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1 * 2^0 = 11$
$(1011)2 = 1 * 2^{-1} + 0 * 2^{-2} + 1 * 2^{-3} + 1 * 2^{-4} = 0.6875$
So, (01011.1011)2 = (11.6875)10.

19. Octal to binary conversion: (24)8 =?
a) (111101)2
b) (010100)2
c) (111100)2
d) (101010)2
View Answer
Answer: b
Explanation: Each digit of the octal number is expressed in terms of group of 3 bits. Thus, the binary equivalent of the octal number is obtained.
(24)8 = (010100)2.

20. Convert binary to octal: (110110001010)2 =?
a) (5512)8
b) (6612)8
c) (4532)8
d) (6745)8
View Answer
Answer: b
Explanation: The binary equivalent is segregated into groups of 3 bits, starting from left. And then for each group, the respective digit is written. Thus, the octal equivalent is obtained.
(110110001010)2 = (6612)8.

21. What is the addition of the binary numbers 11011011010 and 010100101?
a) 0111001000
b) 1100110110
c) 11101111111
d) 10011010011
View Answer
Answer: c
Explanation: The rules for Binary Addition are :
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 (Carry 1)

```
        1

   1 1 0 1 1 0 1 1 0 1 0

 + 0 0 0 1 0 1 0 0 1 0 1
  _____________________
   1 1 1 0 1 1 1 1 1 1 1
  _____________________
```

22. Perform binary addition: 101101 + 011011 = ?
a) 011010
b) 1010100
c) 101110
d) 1001000
View Answer
Answer: d
Explanation:The rules for Binary Addition are :
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 (Carry 1)

```
 1 1 1 1 1 1
   1 0 1 1 0 1
 + 0 1 1 0 1 1
 ______________
 1 0 0 1 0 0 0
 ______________
```

Therefore, the addition of 101101 + 011011 = 1001000.

23. Perform binary subtraction: 101111 – 010101 = ?
a) 100100
b) 010101
c) 011010
d) 011001
View Answer
Answer: c
Explanation: The rules for Binary Subtraction are :
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

```
   1 0 1 1 1 1
 - 0 1 0 1 0 1
  ____________
   0 1 1 0 1 0
  ____________
```

Therefore, The subtraction of 101111 – 010101 = 011010.

24. Binary subtraction of 100101 – 011110 is?
a) 000111
b) 111000
c) 010101
d) 101010
View Answer
Answer: a
Explanation: The rules for Binary Subtraction are :
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

```
   1 0 0 1 0 1
 - 0 1 1 1 1 0
   ___________
   0 0 0 1 1 1
```

```
  _____________
```
Therefore, The subtraction of 100101 – 011110 = 000111.

25. Perform multiplication of the binary numbers: 01001 × 01011 = ?
a) 001100011
b) 110011100
c) 010100110
d) 101010111
View Answer
Answer: a
Explanation: The rules for binary multiplication are:
0 * 0 = 0
0 * 1 = 0
1 * 0 = 0
1 * 1 = 1

```
                0 1 0 0 1
              x 0 1 0 1 1
              _____________
                0 1 0 0 1
              0 1 0 0 1 0
            0 0 0 0 0 0 0
          0 1 0 0 1 0 0 0
        0 0 0 0 0 0 0 0 0
      _____________________
       0 0 1 1 0 0 0 1 1
      _____________________
```
Therefore, 01001 × 01011 = 001100011.

26. 100101 × 0110 = ?
a) 1011001111
b) 0100110011
c) 101111110
d) 0110100101
View Answer
Answer: c
Explanation: The rules for binary multiplication are:
0 * 0 = 0
0 * 1 = 0
1 * 0 = 0
1 * 1 = 1

```
                      1 0 0 1 0 1
                  x       0 1 1 0
                    _____________
                      0 0 0 0 0 0
                    1 0 0 1 0 1 0
                  1 0 0 1 0 1 0 0
                0 0 0 0 0 0 0 0 0
              _____________________
               0 1 1 0 1 1 1 1 0
              _____________________
```
Therefore, 100101 x 0110 = 011011110.

27. On multiplication of (10.10) and (01.01), we get _____
a) 101.0010
b) 0010.101
c) 011.0010
d) 110.0011
View Answer
Answer: c
Explanation: The rules for binary multiplication are:
0 * 0 = 0
0 * 1 = 0

1 * 0 = 0
1 * 1 = 1

```
            1 0.1 0
      x     0 1.0 1

          ___________
            1 0 1 0
          0 0 0 0 0
        1 0 1 0 0 0
      0 0 0 0 0 0 0
    ________________
      0 1 1.0 0 1 0
    ____________________
```

Therefore, 10.10 x 01.01 = 011.0010.

28. Divide the binary numbers: 111101 ÷ 1001 and find the remainder.
a) 0010
b) 1010
c) 1100
d) 0111
View Answer
Answer: d
Explanation: Binary Division is accomplished using long division method.

```
1 0 0 1 ) 1 1 1 1 0 1 ( 1 1
          1 0 0 1

          ___________
          0 1 1 0 0
            1 0 0 1

          ___________
            0 1 1 1
```

Therefore, the remainder of 111101 ÷ 1001 = 0111.

29. Divide the binary number (011010000) by (0101) and find the quotient.
a) 100011
b) 101001
c) 110010
d) 010001
View Answer
Answer: b
Explanation:

```
0 1 0 1 ) 0 1 1 0 1 0 0 0 0 ( 0 1 0 1 1 1
          0 0 0 0

          _____________________
          0 1 1 0 1
          0 0 1 0 1

          _________________
          0 1 0 0 0 0
          0 0 0 0 0 0

          _____________________
              1 0 0 0 0
            0 0 1 0 1

           _________________
              0 1 0 1 1 0
              0 0 0 1 0 1

            _______________
                1 0 0 0 1 0
                0 0 0 1 0 1

          _____________________
                    1 1 1 0 1 0
                    0 0 0 1 0 1

           _____________________
                      1 0 1 0 1
                      0 0 1 0 1
```

```
                  _____________________
                      1 0 0 0 0
```

Therefore, the quotient of 011010000 ÷ 1001 = 101001.

30. Binary subtraction of 101101 – 001011 = ?
a) 100010
b) 010110
c) 110101
d) 101100
View Answer
Answer: a
Explanation: The rules for binary subtraction are:
0 – 0 = 0
0 – 1 = 1 (Borrow 1)
1 – 0 = 1
1 – 1 = 0

```
  1 0 1 1 0 1
- 0 0 1 0 1 1

  1 0 0 0 1 0
  _____________
```

Therefore, the subtraction of 101101 – 001011 = 100010.

31. 1’s complement of 1011101 is _____
a) 0101110
b) 1001101
c) 0100010
d) 1100101
View Answer
Answer: c
Explanation: 1’s complement of a binary number is obtained by reversing the binary bits. All the 1’s to 0’s and 0’s to 1’s.
Thus, 1’s complement of 1011101 = 0100010.

32. 2’s complement of 11001011 is _____
a) 01010111
b) 11010100
c) 00110101
d) 11100010
View Answer
Answer: c
Explanation: 2’s complement of a binary number is obtained by finding the 1’s complement of the number and then adding 1 to it.
2’s complement of 11001011 = 00110100 + 1 = 00110101.

33. On subtracting (01010)2 from (11110)2 using 1’s complement, we get _____
a) 01001
b) 11010
c) 10101
d) 10100
View Answer
Answer: d
Explanation: Steps For Subtraction using 1’s complement are:
-> 1’s complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and 1 is added to the last bit of the result.
-> Else, if there is no carry, then 1’s complement of the result is found out and a ‘-’ sign preceeds the result.

```
                                      1 1 1
                    Minuend -         1 1 1 1 0
1’s complement of subtrahend -        1 0 1 0 1

                                      ___________
                 Carry over -    1    1 0 0 1 1
                                             1

                                      ___________
                                      1 0 1 0 0
```

34. On subtracting (010110)2 from (1011001)2 using 2's complement, we get _____
a) 0111001
b) 1100101
c) 0110110
d) 1000011
View Answer
Answer: d
Explanation: Steps For Subtraction using 2's complement are:
-> 2's complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and the result is positive.
-> Else, if there is no carry, then 2's complement of the result is found out and a '-' sign preceeds the result.

```
      1's complement of subtrahend -              1 1 0 1 0 0 1
                                                  _____________
                                                  1 1 1
                          Minuend -               1 0 1 1 0 0 1
      2's complement of subtrahend -              1 1 0 1 0 1 0
                                                  _____________

                       Carry over -    1          1 0 0 0 0 1 1

Answer: 1000011
```

35. On subtracting (001100)2 from (101001)2 using 2's complement, we get _____
a) 1101100
b) 011101
c) 11010101
d) 11010111
View Answer
Answer: b
Explanation: Steps For Subtraction using 2's complement are:
-> 2's complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and the result is positive.
-> Else, if there is no carry, then 2's complement of the result is found out and a '-' sign preceeds the result.

36. On addition of 28 and 18 using 2's complement, we get _____
a) 00101110
b) 0101110
c) 00101111
d) 1001111
View Answer
Answer: b
Explanation: Steps for Binary Addition Using 2's complement:
-> The binary equivalent of the two numbers are obtained and added using the rules of binary addition.

```
Augend -         0   0 1 1 1 0 0

Addend -         0   0 1 0 0 1 0
                 _______________
                 0   1 0 1 1 1 0


Answer: 0  1 0 1 1 1 0
```

37. On addition of +38 and -20 using 2's complement, we get _____
a) 11110001
b) 100001110
c) 010010
d) 110101011
View Answer
Answer: c
Explanation: Steps for Binary Addition Using 2's complement:
-> The 2's complement of the addend is found out and added to the first number.
-> The result is the 2's complement of the sum obtained.

```
                      Augend -           0 1 0 0 1 1 0
2's Complement of Subtrahend:            1 1 0 1 1 0 0
                                         _____________
```

```
                                1          0 0 1 0 0 1 0

Answer: 0 1 0 0 1 0
```

38. On addition of -46 and +28 using 2’s complement, we get _____
a) -10010
b) -00101
c) 01011
d) 0100101
View Answer
Answer: a
Explanation: The BCD form is written of the two given numbers, in their signed form. After which, normal binary addition is performed.
Augend is 28 and Subtrahend is -46.

```
                             Augend -           0 0 1 1 1 0 0   .....(a)
      2’s Complement of Subtrahend:             1 0 1 0 0 1 0   .....(b)

                                                _______________
               Addiing (a) and (b):             1 1 0 1 1 1 0
Since, there is no carry, so answer will be negative
and 2's complement of the above result is determined.
                                                  0 0 1 0 0 0 1
                                              +               1
                                                 _____________
                                                  0 0 1 0 0 1 0


Answer: - 1 0 0 1 0
```

39. On addition of -33 and -40 using 2’s complement, we get _____
a) 1001110
b) -110101
c) 0110001
d) -1001001
View Answer
Answer: d
Explanation: The BCD form is written of the two given numbers, in their signed form. After which, normal binary addition is performed.
Augend is -40 and Subtrahend is -33.

```
                             Augend -           1    0 1 0 0 0 0 1
.....(a)
      2’s Complement of Subtrahend:             1    1 0 1 1 0 0 1
.....(b)

                                                ____________________
               Addiing (a) and (b):             1 0   1 0 0 1 0 0 0
Since, there is no carry, so answer will be negative
and 2's complement of the above result is determined.
                                                  1 0 0 1 0 0 0
                                              +               1
                                                 _____________
                                                  1 0 0 1 0 0 1
 Answer: -1001001
```

40. On subtracting +28 from +29 using 2’s complement, we get _____
a) 11111010
b) 111111001
c) 100001
d) 1
View Answer
Answer: d
Explanation: Steps For Subtraction using 2’s complement are:
-> 2’s complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and the result is positive.
-> Else, if there is no carry, then 2’s complement of the result is found out and a ‘-’ sign preceeds the result.

```
         1’s complement of subtrahend -         1 0 0 0 1 1
```

```
                          Minuend -         0 1 1 1 0 1
        2's complement of subtrahend -        1 0 0 1 0 0
                                            ____________________

                        Carry over -    1   0 0 0 0 0 1

Answer: 000001 = 1
```

41. If the number of bits in the sum exceeds the number of bits in each added numbers, it results in _____
a) Successor
b) Overflow
c) Underflow
d) Predecessor
View Answer
Answer: b
Explanation: If the number of bits in the sum exceeds the number of bits in each added numbers, it results in overflow and is also known as excess-one. In case of any arithmetic operation, if the result has less number of bits than the operands, then it is known as underflow condition.

42. An overflow is a _____
a) Hardware problem
b) Software problem
c) User input problem
d) Input Output Error
View Answer
Answer: b
Explanation: An overflow is a software problem which occurs when the processor cannot handle the result properly when it produces an out of the range output.

43. An overflow occurs in _____
a) MSD position
b) LSD position
c) Middle position
d) Signed Bit
View Answer
Answer: a
Explanation: An overflow occurs at the Most Significant Digit position. It occurs when the processor cannot handle the result properly when it produces an out of the range output.

44. Logic circuitry is used to detect _____
a) Underflow
b) MSD
c) Overflow
d) LSD
View Answer
Answer: c
Explanation: To check the overflow logic circuitry is used in each case. Overflow occurs when the processor cannot handle the result properly when it produces an out of the range output.

45. 1's complement can be easily obtained by using _____
a) Comparator
b) Inverter
c) Adder
d) Subtractor
View Answer
Answer: b
Explanation: With the help of inverter the 1's complement is easily obtained. Since, during the operation of 1's complement 1 is converted into 0 and vice-versa and this is well suited for the inverter.

46. Binary coded decimal is a combination of _____
a) Two binary digits
b) Three binary digits
c) Four binary digits
d) Five binary digits
View Answer

Answer: c
Explanation: Binary coded decimal is a combination of 4 binary digits. For example-8421.

47. The decimal number 10 is represented in its BCD form as _____
a) 10100000
b) 01010111
c) 00010000
d) 00101011
View Answer

Answer: c
Explanation: The decimal number 10 is represented in its BCD form as 0001 0000, in accordance to 8421 for each of the two digits.

48. Add the two BCD numbers: 1001 + 0100 = ?
a) 10101111
b) 01010000
c) 00010011
d) 00101011
View Answer

Answer: c
Explanation: Firstly, Add the 1001 and 0100. We get 1101 as output but it's not in BCD form. So, we add 0110 (i.e. 6) with 1101. As a result we get 10011 and it's BCD form is 0001 0011.

49. Carry out BCD subtraction for (68) – (61) using 10's complement method.
a) 00000111
b) 01110000
c) 100000111
d) 011111000
View Answer
Answer: a
Explanation: First the two numbers are converted into their respective BCD form using 8421 sequence. Then binary subtraction is carried out.

50. Code is a symbolic representation of _____ information.
a) Continuous
b) Discrete
c) Analog
d) Both continuous and discrete
View Answer
Answer: b
Explanation: Code is a symbolic representation of discrete information, which may be present in the form of numbers, letters or physical quantities. Mostly, it is represented using a particular number system like decimal or binary and such like.

51. When numbers, letters or words are represented by a special group of symbols, this process is called _____
a) Decoding
b) Encoding
c) Digitizing
d) Inverting
View Answer
Answer: b
Explanation: When numbers, letters or words are represented by a special group of symbols, this process is called encoding. Encoding in the sense of fetching the codes or words in a computer. It is done to secure the transmission of information.

52. A three digit decimal number requires _____ for representation in the conventional BCD format.
a) 3 bits
b) 6 bits
c) 12 bits
d) 24 bits
View Answer
Answer: c
Explanation: The number of bits needed to represent a given decimal number is always greater than the number

of bits required for a straight binary encoding of the same. Hence, a three digit decimal number requires 12 bits for representation in BCD format.

53. How many bits would be required to encode decimal numbers 0 to 9999 in straight binary codes?
a) 12
b) 14
c) 16
d) 18
View Answer
Answer: b
Explanation: Total number of decimals to be represented = 10000 = 10^4 = 2^n (where n is the number of bits required) = $2^{13.29}$. Therefore, the number of bits required for straight binary encoding = 14.

54. The excess-3 code for 597 is given by _____
a) 100011001010
b) 100010100111
c) 010110010111
d) 010110101101
View Answer
Answer: a
Explanation: The addition of '3' to each digit yields the three new digits '8', '12' and '10'. Hence, the corresponding four-bit binary equivalents are 100011001010, in accordance to 8421 format.

55. The decimal equivalent of the excess-3 number 110010100011.01110101 is _____
a) 970.42
b) 1253.75
c) 861.75
d) 1132.87
View Answer
Answer: a

56. In boolean algebra, the OR operation is performed by which properties?
a) Associative properties
b) Commutative properties
c) Distributive properties
d) All of the Mentioned
View Answer
Answer: d
Explanation: The expression for Associative property is given by A+(B+C) = (A+B)+C & A*(B*C) = (A*B)*C.
The expression for Commutative property is given by A+B = B+A & A*B = B*A.
The expression for Distributive property is given by A+BC=(A+B)(A+C) & A(B+C) = AB+AC.

57. The expression for Absorption law is given by _____
a) A + AB = A
b) A + AB = B
c) AB + AA' = A
d) A + B = B + A
View Answer
Answer: a
Explanation: The expression for Absorption Law is given by: A+AB = A.
Proof: A + AB = A(1+B) = A (Since 1 + B = 1 as per 1's Property).

58. According to boolean law: A + 1 = ?
a) 1
b) A
c) 0
d) A'
View Answer
Answer: a
Explanation: A + 1 = 1, as per 1's Property.

59. The involution of A is equal to _____
a) A
b) A'
c) 1
d) 0
View Answer

Answer: a
Explanation: The involution of A means double inversion of A (i.e. A") and is equal to A.
Proof: ((A)')' = A

60. A(A + B) = ?
a) AB
b) 1
c) (1 + AB)
d) A
View Answer
Answer: d
Explanation: A(A + B) = AA + AB (By Distributive Property) = A + AB (A.A = A By Commutative Property) = A(1 + B) = A*1 (1 + B = 1 by 1's Property) = A.

61. DeMorgan's theorem states that _____
a) (AB)' = A' + B'
b) (A + B)' = A' * B
c) A' + B' = A'B'
d) (AB)' = A' + B
View Answer
Answer: a
Explanation: The DeMorgan's law states that (AB)' = A' + B' & (A + B)' = A' * B', as per the Dual Property.

62. (A + B)(A' * B') = ?
a) 1
b) 0
c) AB
d) AB'
View Answer
Answer: b
Explanation: The DeMorgan's law states that (AB)' = A' + B' & (A + B)' = A' * B', as per the Dual Property.

63. Complement of the expression A'B + CD' is _____
a) (A' + B)(C' + D)
b) (A + B')(C' + D)
c) (A' + B)(C' + D)
d) (A + B')(C + D')
View Answer
Answer: b
Explanation: (A'B + CD')' = (A'B)'(CD')' (By DeMorgan's Theorem) = (A" + B')(C' + D") (By DeMorgan's Theorem) = (A + B')(C' + D).

64. Simplify Y = AB' + (A' + B)C.
a) AB' + C
b) AB + AC
c) A'B + AC'
d) AB + A
View Answer
Answer: a
Explanation: Y = AB' + (A' + B)C = AB' + (AB')'C = (AB' + C)(AB' + AB') = (AB' + C).1 = (AB' + C).

65. The boolean function A + BC is a reduced form of _____
a) AB + BC
b) (A + B)(A + C)
c) A'B + AB'C
d) (A + C)B
View Answer
Answer: b
Explanation: (A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC (By Commutative Property) = A(1 + C + B) + BC = A + BC (1 + B + C =1 By 1's Property).

66. In boolean algebra, the OR operation is performed by which properties?
a) Associative properties
b) Commutative properties
c) Distributive properties
d) All of the Mentioned
View Answer

Answer: d
Explanation: The expression for Associative property is given by A+(B+C) = (A+B)+C & A*(B*C) = (A*B)*C.
The expression for Commutative property is given by A+B = B+A & A*B = B*A.
The expression for Distributive property is given by A+BC=(A+B)(A+C) & A(B+C) = AB+AC.

67. The expression for Absorption law is given by _____
a) A + AB = A
b) A + AB = B
c) AB + AA' = A
d) A + B = B + A
View Answer
Answer: a
Explanation: The expression for Absorption Law is given by: A+AB = A.
Proof: A + AB = A(1+B) = A (Since 1 + B = 1 as per 1's Property).

68. According to boolean law: A + 1 = ?
a) 1
b) A
c) 0
d) A'
View Answer
Answer: a
Explanation: A + 1 = 1, as per 1's Property.

69. The involution of A is equal to _____
a) A
b) A'
c) 1
d) 0
View Answer
Answer: a
Explanation: The involution of A means double inversion of A (i.e. A") and is equal to A.
Proof: ((A)')' = A

70. A(A + B) = ?
a) AB
b) 1
c) (1 + AB)
d) A
View Answer
Answer: d
Explanation: A(A + B) = AA + AB (By Distributive Property) = A + AB (A.A = A By Commutative Property) = A(1 + B) = A*1 (1 + B = 1 by 1's Property) = A.

71. DeMorgan's theorem states that _____
a) (AB)' = A' + B'
b) (A + B)' = A' * B
c) A' + B' = A'B'
d) (AB)' = A' + B
View Answer
Answer: a
Explanation: The DeMorgan's law states that (AB)' = A' + B' & (A + B)' = A' * B', as per the Dual Property.

72. (A + B)(A' * B') = ?
a) 1
b) 0
c) AB
d) AB'
View Answer
Answer: b
Explanation: The DeMorgan's law states that (AB)' = A' + B' & (A + B)' = A' * B', as per the Dual Property.

73. Complement of the expression A'B + CD' is _____
a) (A' + B)(C' + D)
b) (A + B')(C' + D)
c) (A' + B)(C' + D)

d) (A + B')(C + D')
View Answer
Answer: b
Explanation: (A'B + CD')' = (A'B)'(CD')' (By DeMorgan's Theorem) = (A" + B')(C' + D") (By DeMorgan's Theorem) = (A + B')(C' + D).

74. Simplify Y = AB' + (A' + B)C.
a) AB' + C
b) AB + AC
c) A'B + AC'
d) AB + A
View Answer
Answer: a
Explanation: Y = AB' + (A' + B)C = AB' + (AB')'C = (AB' + C)(AB' + AB') = (AB' + C).1 = (AB' + C).

75. The boolean function A + BC is a reduced form of _____
a) AB + BC
b) (A + B)(A + C)
c) A'B + AB'C
d) (A + C)B
View Answer
Answer: b
Explanation: (A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC (By Commutative Property) = A(1 + C + B) + BC = A + BC (1 + B + C =1 By 1's Property).

76. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
a) Venn Diagram
b) Cycle Diagram
c) Block diagram
d) Triangular Diagram
View Answer
Answer: a
Explanation: A Karnaugh map (K-map) is an abstract form of Venn diagram organized as a matrix of squares, where each square represents a Maxterm or a Minterm.

77. There are _____ cells in a 4-variable K-map.
a) 12
b) 16
c) 18
d) 8
View Answer
Answer: b
Explanation: There are 16 = (2^4) cells in a 4-variable K-map.

78. The K-map based Boolean reduction is based on the following Unifying Theorem: A + A' = 1.
a) Impact
b) Non Impact
c) Force
d) Complementarity
View Answer
Answer: b
Explanation: The given expression A +A' = 1 is based on non-impact unifying theorem.

79. Each product term of a group, w'.x.y' and w.y, represents the _____ in that group.
a) Input
b) POS
c) Sum-of-Minterms
d) Sum of Maxterms
View Answer
Answer: c
Explanation: In a minterm, each variable w, x or y appears once either as the variable itself or as the inverse. So, the given expression satisfies the property of Sum of Minterm.

80. The prime implicant which has at least one element that is not present in any other implicant is known as _____
a) Essential Prime Implicant
b) Implicant

c) Complement
d) Prime Complement
View Answer
Answer: a
Explanation: Essential prime implicants are prime implicants that cover an output of the function that no combination of other prime implicants is able to cover.

81. Product-of-Sums expressions can be implemented using _____
a) 2-level OR-AND logic circuits
b) 2-level NOR logic circuits
c) 2-level XOR logic circuits
d) Both 2-level OR-AND and NOR logic circuits
View Answer
Answer: d
Explanation: Product-of-Sums expressions can be implemented using 2-level OR-AND & NOR logic circuits.

82. Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given _____
a) Function
b) Value
c) Set
d) Word
View Answer
Answer: a
Explanation: Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given function.

83. Don’t care conditions can be used for simplifying Boolean expressions in _____
a) Registers
b) Terms
c) K-maps
d) Latches
View Answer
Answer: c
Explanation: Don’t care conditions can be used for simplifying Boolean expressions in K-maps which helps in pairing with 1/0.

84. It should be kept in mind that don’t care terms should be used along with the terms that are present in _____
a) Minterms
b) Expressions
c) K-Map
d) Latches
View Answer
Answer: a
Explanation: It should be kept in mind that don’t care terms should be used along with the terms that are present in minterms as well as maxterms which reduces the complexity of the boolean expression.

85. Using the transformation method you can realize any POS realization of OR-AND with only.
a) XOR
b) NAND
c) AND
d) NOR
View Answer
Answer: d
Explanation: Using the transformation method we can realize any POS realization of OR-AND with only NOR.

86. There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations.
a) X-NOR
b) XOR
c) NOR
d) NAND
View Answer
Answer: a
Explanation: There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and XNOR operations.

Expression of XOR : AB’ + A’B
Expression of XNOR : AB + A’B’

87. These logic gates are widely used in _____ design and therefore are available in IC form.
a) Sampling
b) Digital
c) Analog
d) Systems
View Answer
Answer: b
Explanation: These logic gates(XOR, XNOR, NOR) are widely used in digital design and therefore are available in IC form as digital circuits deal with data transmission in the form of binary digits.

88. In case of XOR/XNOR simplification we have to look for the following _____
a) Diagonal Adjacencies
b) Offset Adjacencies
c) Straight Adjacencies
d) Both diagonal and offset adjencies
View Answer
Answer: d
Explanation: In case of XOR/XNOR simplification we have to look for the following diagonal and offset adjacencies. XOR gives output 1 when odd number of 1s are present in input while XNOR gives output 1 when even number of 1s or all 0s are present in input.

88. Entries known as _____ mapping.
a) Diagonal
b) Straight
c) K
d) Boolean
View Answer
Answer: a
Explanation: Entries known as diagonal mapping. The diagonal mapping holds true when for any relation, there is a projection of product on the factor.

89. What is a multiplexer?
a) It is a type of decoder which decodes several inputs and gives one output
b) A multiplexer is a device which converts many signals into one
c) It takes one input and results into many output
d) It is a type of encoder which decodes several inputs and gives one output
View Answer
Answer: b
Explanation: A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

90. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
a) Data Selector
b) Data distributor
c) Both data selector and data distributor
d) DeMultiplexer
View Answer
Answer: a
Explanation: Data Selector is another name of Multiplexer. A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

91. It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of _____
a) Inputs
b) Outputs
c) Selection lines
d) Enable lines
View Answer
Answer: a
Explanation: It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of inputs.

92. Which is the major functioning responsibility of the multiplexing combinational circuit?
a) Decoding the binary information
b) Generation of all minterms in an output function with OR-gate
c) Generation of selected path between multiple sources and a single destination
d) Encoding of binary information
View Answer
Answer: c
Explanation: The major functioning responsibility of the multiplexing combinational circuit is generation of selected path between multiple sources and a single destination because it makes the circuit too flexible. A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

93. What is the function of an enable input on a multiplexer chip?
a) To apply Vcc
b) To connect ground
c) To active the entire chip
d) To active one half of the chip
View Answer
Answer: c
Explanation: Enable input is used to active the chip, when enable is high the chip works (ACTIVE), when enable is low the chip does not work (MEMORY). However, Enable can be Active-High or Active-Low, indicating it is active either when it is connected to VCC or GND respectively.

94. One multiplexer can take the place of _____
a) Several SSI logic gates
b) Combinational logic circuits
c) Several Ex-NOR gates
d) Several SSI logic gates or combinational logic circuits
View Answer
Answer: d
Explanation: A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines. Since many operational behaviour can be performed by using a multiplexer. Whereas, a combinational circuit is a combination of many logic gates which makes the circuit more complex.

95. A digital multiplexer is a combinational circuit that selects _____
a) One digital information from several sources and transmits the selected one
b) Many digital information and convert them into one
c) Many decimal inputs and transmits the selected information
d) Many decimal outputs and accepts the selected information
View Answer
Answer: a
Explanation: A digital multiplexer is a combinational circuit that selects one digital information from several sources and transmits the selected information on a single output line depending on the status of the select lines. That is why it is also known as a data selector.

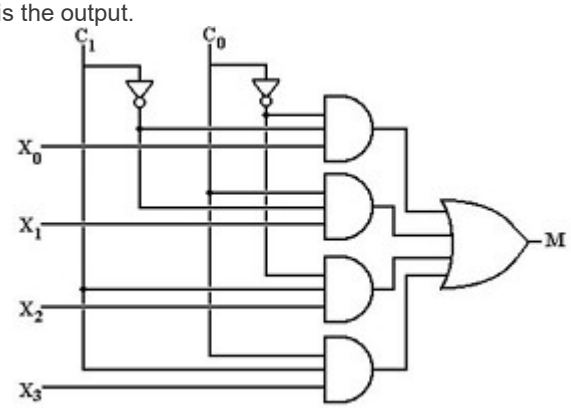
96. In a multiplexer, the selection of a particular input line is controlled by _____
a) Data controller
b) Selected lines
c) Logic gates
d) Both data controller and selected lines
View Answer
Answer: b
Explanation: The selection of a particular input line is controlled by a set of selected lines in a multiplexer, which helps to select a particular input from several sources.

97. If the number of n selected input lines is equal to 2^m then it requires _____ select lines.
a) 2
b) m
c) n
d) 2^n
View Answer
Answer: b
Explanation: If the number of n selected input lines is equal to 2^m then it requires m select lines to select one of m select lines.

98. How many select lines would be required for an 8-line-to-1-line multiplexer?
a) 2
b) 4
c) 8
d) 3
View Answer
Answer: d
Explanation: 2^n input lines, n control lines and 1 output line available for MUX. Here, 8 input lines mean 2^3 inputs. So, 3 control lines are possible. Depending on the status of the select lines, the input is selected and fed to the output.

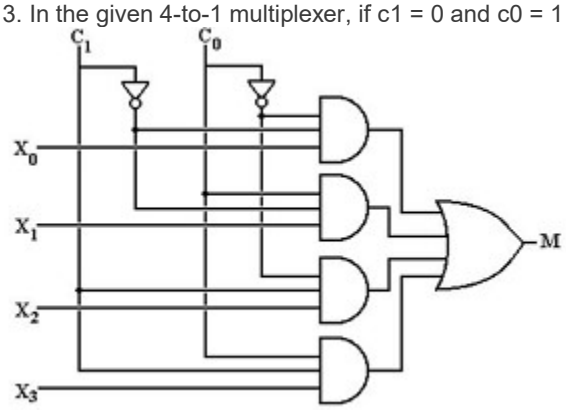
99. A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay
b) DPDT switch
c) Rotary switch
d) Linear stepper
View Answer
Answer: c
Explanation: A basic multiplexer principle can be demonstrated through the use of a rotary switch. Since its behaviour is similar to the multiplexer. There are around 10 digits out of which one is selected one at a time and fed to the output.

100. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
a) 3
b) 4
c) 2
d) 5
View Answer
Answer: c
Explanation: There are two NOT gates required for the construction of 4-to-1 multiplexer. x0, x1, x2 and x3 are the inputs and C1 and C0 are the select lines and M is the output.



The diagram of a 4-to-1 multiplexer is shown below:

13. In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is _____



a) X0
b) X1
c) X2
d) X3
View Answer

Answer: b
Explanation: The output will be X1, because c1 = 0 and c0 = 1 results into 1 which further results as X1. And rest of the AND gates gives output as 0.

101. The enable input is also known as _____
a) Select input
b) Decoded input
c) Strobe
d) Sink
View Answer
Answer: c
Explanation: The enable input is also known as strobe which is used to cascade two or more multiplexer ICs to construct a multiplexer with a larger number of inputs. Enable input activates the multiplexer to operate.

102. In parts of the processor, adders are used to calculate _____
a) Addresses
b) Table indices
c) Increment and decrement operators
d) All of the Mentioned
View Answer
Answer: d
Explanation: Adders are used to perform the operation of addition. Thus, in parts of the processor, adders are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

103. Total number of inputs in a half adder is _____
a) 2
b) 3
c) 4
d) 1
View Answer
Answer: a
Explanation: Total number of inputs in a half adder is two. Since an EXOR gates has 2 inputs and carry is connected with the input of EXOR gates. The output of half-adder is also 2, them being, SUM and CARRY. The output of EXOR gives SUM and that of AND gives carry.

104. In which operation carry is obtained?
a) Subtraction
b) Addition
c) Multiplication
d) Both addition and subtraction
View Answer
Answer: b
Explanation: In addition, carry is obtained. For example: 1 0 1 + 1 1 1 = 1 0 0; in this example carry is obtained after 1st addition (i.e. 1 + 1 = 1 0). In subtraction, borrow is obtained. Like, 0 – 1 = 1 (borrow 1).

105. If A and B are the inputs of a half adder, the sum is given by _____
a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B
View Answer
Answer: c
Explanation: If A and B are the inputs of a half adder, the sum is given by A XOR B, while the carry is given by A AND B.

106. If A and B are the inputs of a half adder, the carry is given by _____
a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B
View Answer
Answer: a
Explanation: If A and B are the inputs of a half adder, the carry is given by: A(AND)B, while the sum is given by A XOR B.

107. Half-adders have a major limitation in that they cannot _____
a) Accept a carry bit from a present stage

b) Accept a carry bit from a next stage
c) Accept a carry bit from a previous stage
d) Accept a carry bit from the following stages
View Answer
Answer: c
Explanation: Half-adders have a major limitation in that they cannot accept a carry bit from a previous stage, meaning that they cannot be chained together to add multi-bit numbers. However, the two output bits of a half-adder can also represent the result A+B=3 as sum and carry both being high.

108.The difference between half adder and full adder is _____
a) Half adder has two inputs while full adder has four inputs
b) Half adder has one output while full adder has two outputs
c) Half adder has two inputs while full adder has three inputs
d) All of the Mentioned
View Answer
Answer: c
Explanation: Half adder has two inputs while full adder has three outputs; this is the difference between them, while both have two outputs SUM and CARRY.

109. If A, B and C are the inputs of a full adder then the sum is given by _____
a) A AND B AND C
b) A OR B AND C
c) A XOR B XOR C
d) A OR B OR C
View Answer
Answer: c
Explanation: If A, B and C are the inputs of a full adder then the sum is given by A XOR B XOR C.

110. If A, B and C are the inputs of a full adder then the carry is given by _____
a) A AND B OR (A OR B) AND C
b) A OR B OR (A AND B) C
c) (A AND B) OR (A AND B)C
d) A XOR B XOR (A XOR B) AND C
View Answer
Answer: a
Explanation: If A, B and C are the inputs of a full adder then the carry is given by A AND B OR (A OR B) AND C, which is equivalent to (A AND B) OR (B AND C) OR (C AND A).

111. How many AND, OR and EXOR gates are required for the configuration of full adder?
a) 1, 2, 2
b) 2, 1, 2
c) 3, 1, 2
d) 4, 0, 1
View Answer
Answer: b
Explanation: There are 2 AND, 1 OR and 2 EXOR gates required for the configuration of full adder, provided using half adder. Otherwise, configuration of full adder would require 3 AND, 2 OR and 2 EXOR.

112. In digital logic, a counter is a device which _____
a) Counts the number of outputs
b) Stores the number of times a particular event or process has occurred
c) Stores the number of times a clock pulse rises and falls
d) Counts the number of inputs
View Answer
Answer: b
Explanation: In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

113. A counter circuit is usually constructed of _____
a) A number of latches connected in cascade form
b) A number of NAND gates connected in cascade form
c) A number of flip-flops connected in cascade
d) A number of NOR gates connected in cascade form
View Answer
Answer: c
Explanation: A counter circuit is usually constructed of a number of flip-flops connected in cascade. Preferably, JK Flip-flops are used to construct counters and registers.

114. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of ‘n’ number of flip-flops?
a) 0 to 2^n
b) 0 to $2^n + 1$
c) 0 to $2^n – 1$
d) 0 to $2^{n+1/2}$
View Answer
Answer: c
Explanation: The maximum possible range of bit-count specifically in n-bit binary counter consisting of ‘n’ number of flip-flops is 0 to 2^n-1. For say, there is a 2-bit counter, then it will count till 2^2-1 = 3. Thus, it will count from 0 to 3.

115. How many types of the counter are there?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: b
Explanation: Counters are of 3 types, namely, (i)asynchronous/synchronous, (ii)single and multi-mode & (iii)modulus counter. These further can be subdivided into Ring Counter, Johnson Counter, Cascade Counter, Up/Down Counter and such like.

116. A decimal counter has _____ states.
a) 5
b) 10
c) 15
d) 20
View Answer
Answer: b
Explanation: Decimal counter is also known as 10 stage counter. So, it has 10 states. It is also known as Decade Counter counting from 0 to 9.

117. Ripple counters are also called _____
a) SSI counters
b) Asynchronous counters
c) Synchronous counters
d) VLSI counters
View Answer
Answer: b
Explanation: Ripple counters are also called asynchronous counter. In Asynchronous counters, only the first flip-flop is connected to an external clock while the rest of the flip-flops have their preceding flip-flop output as clock to them.

118. Synchronous counter is a type of _____
a) SSI counters
b) LSI counters
c) MSI counters
d) VLSI counters
View Answer
Answer: c
Explanation: Synchronous Counter is a Medium Scale Integrated (MSI). In Synchronous Counters, the clock pulse is supplied to all the flip-flops simultaneously.

119. Three decade counter would have _____
a) 2 BCD counters
b) 3 BCD counters
c) 4 BCD counters
d) 5 BCD counters
View Answer
Answer: b
Explanation: Three decade counter has 30 states and a BCD counter has 10 states. So, it would require 3 BCD counters. Thus, a three decade counter will count from 0 to 29.

120. BCD counter is also known as _____
a) Parallel counter
b) Decade counter

c) Synchronous counter
d) VLSI counter
View Answer
Answer: b
Explanation: BCD counter is also known as decade counter because both have the same number of stages and both count from 0 to 9.

121. The parallel outputs of a counter circuit represent the _____
a) Parallel data word
b) Clock frequency
c) Counter modulus
d) Clock count
View Answer
Answer: d
Explanation: The parallel outputs of a counter circuit represent the clock count. A counter counts the number of times an event takes place in accordance to the clock pulse.

122. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?
a) Ring shift
b) Clock
c) Johnson
d) Binary
View Answer
Answer: a
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. Thus, it generates equally spaced timing pulses.

123. A bidirectional 4-bit shift register is storing the nibble 1101. Its input is HIGH. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____
a) 1101
b) 0111
c) 0001
d) 1110
View Answer
Answer: b
Explanation: Mode is high means it's a right shift register. Then after 3 clock pulses enter bits are 011 and remained bit in register is 1. Therefore, 0111 is the required solution.
1011 | 1101
101 | 1110 -> 1st clock pulse
10 | 1111 -> 2nd clock pulse
1 | 0111 -> 3rd clock pulse.

124. To operate correctly, starting a ring shift counter requires _____
a) Clearing all the flip-flops
b) Presetting one flip-flop and clearing all others
c) Clearing one flip-flop and presetting all others
d) Presetting all the flip-flops
View Answer
Answer: b
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. To operate correctly, starting a ring shift counter requires presetting one flip-flop and clearing all others so that it can shift to the next bit.

125. A 4-bit shift register that receives 4 bits of parallel data will shift to the _____ by _____ position for each clock pulse.
a) Right, one
b) Right, two
c) Left, one
d) Left, three
View Answer
Answer: a
Explanation: If register shifts towards left then it shift by a bit to the left and if register shifts right then it shift to the right by one bit. Since, it receives parallel data, then by default, it will shift to right by one position.

126. How many clock pulses will be required to completely load serially a 5-bit shift register?
a) 2
b) 3

c) 4
d) 5
View Answer
Answer: d
Explanation: A register is a collection of FFS. To load a bit, we require 1 clock pulse for 1 shift register. So, for 5-bit shift register we would require of 5 clock pulses.

127. How is a strobe signal used when serially loading a shift register?
a) To turn the register on and off
b) To control the number of clocks
c) To determine which output Qs are used
d) To determine the FFs that will be used
View Answer
Answer: b
Explanation: A strobe is used to validate the availability of data on the data line. It (an auxiliary signal used to help synchronize the real data in an electrical bus when the bus components have no common clock) signal is used to control the number of clocks during serially loading a shift register.

128. An 8-bit serial in/serial out shift register is used with a clock frequency of 150 kHz. What is the time delay between the serial input and the Q3 output?
a) 1.67 s
b) 26.67 s
c) 26.7 ms
d) 267 ms
View Answer
Answer: b
Explanation: In serial-sifting, one bit of data is shifted one at a time. From Q0 to Q3 total of 4 bit shifting takes place. Therefore, 4/150kHz = 26.67 microseconds.

129. What are the three output conditions of a three-state buffer?
a) HIGH, LOW, float
b) High-Z, 0, float
c) Negative, positive, 0
d) 1, Low-Z, float
View Answer
Answer: a
Explanation: Three conditions of a three-state buffer are HIGH, LOW & float.

130. The primary purpose of a three-state buffer is usually _____
a) To provide isolation between the input device and the data bus
b) To provide the sink or source current required by any device connected to its output without loading down the output device
c) Temporary data storage
d) To control data flow
View Answer
Answer: a
Explanation: The primary purpose of a three-state buffer is usually to provide isolation between the input device or peripheral devices and the data bus. Three conditions of a three-state buffer are HIGH, LOW & float.

131. What is the difference between a ring shift counter and a Johnson shift counter?
a) There is no difference
b) A ring is faster
c) The feedback is reversed
d) The Johnson is faster
View Answer
Answer: c

132. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: c
Explanation: The registers in which data can be shifted serially or parallelly are known as shift registers. Based

on how binary information is entered or shifted out, shift registers are classified into 4 categories, viz., Serial-In/Serial-Out(SISO), Serial-In/Parallel-Out (SIPO), Parallel-In/Serial-Out (PISO), Parallel-In/Parallel-Out (PIPO).

133. The full form of SIPO is _____
a) Serial-in Parallel-out
b) Parallel-in Serial-out
c) Serial-in Serial-out
d) Serial-In Peripheral-Out
View Answer
Answer: a
Explanation: SIPO is always known as Serial-in Parallel-out.

134. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
a) Tristate
b) End around
c) Universal
d) Conversion
View Answer
Answer: c
Explanation: A shift register can shift it's data either left or right. The universal shift register is capable of shifting data left, right and parallel load capabilities.

135. How can parallel data be taken out of a shift register simultaneously?
a) Use the Q output of the first FF
b) Use the Q output of the last FF
c) Tie all of the Q outputs together
d) Use the Q output of each FF
View Answer
Answer: d
Explanation: Because no other flip-flops are connected with the output Q, therefore one can use the Q out of each FF to take out parallel data.

136. What is meant by the parallel load of a shift register?
a) All FFs are preset with data
b) Each FF is loaded with data, one at a time
c) Parallel shifting of data
d) All FFs are set with data
View Answer
Answer: a
Explanation: At Preset condition, outputs of flip-flops will be 1. Preset = 1 means Q = 1, thus input is definitely 1.

137. The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____
a) 01110
b) 00001
c) 00101
d) 00110
View Answer
Answer: c
Explanation: LSB bit is inverted and feed back to MSB:
01110->initial
10111->first clock pulse
01011->second
00101->third.

138. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)
a) 1100
b) 0011
c) 0000
d) 1111
View Answer
Answer: c
Explanation: In Serial-In/Serial-Out shift register, data will be shifted one at a time with every clock pulse. Therefore,
Wait | Store

1100 | 0000
110 | 0000 1st clock
11 | 0000 2nd clock.

139. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____
a) 0000
b) 1111
c) 0111
d) 1000
View Answer
Answer: c
Explanation: In Serial-In/Parallel-Out shift register, data will be shifted all at a time with every clock pulse. Therefore,
Wait | Store
0111 | 0000
011 | 1000 1st clk
01 | 1100 2nd clk
0 | 1110 3rd clk
X | 1111 4th clk.

140. With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in _____
a) 4 μs
b) 40 μs
c) 400 μs
d) 40 ms
View Answer
Answer: b
Explanation: f = 200 KHZ; T = (1/200) m sec = (1/0.2) micro-sec = 5 micro-sec;
In serial transmission, data enters one bit at a time. After 8 clock cycles only 8 bit will be loaded = 8 * 5 = 40 micro-sec.

141. An 8-bit serial in/serial out shift register is used with a clock frequency of 2 MHz to achieve a time delay (td) of _____
a) 16 us
b) 8 us
c) 4 us
d) 2 us
View Answer
Answer: c

142. Modulus refers to _____
a) A method used to fabricate decade counter units
b) The modulus of elasticity, or the ability of a circuit to be stretched from one mode to another
c) An input on a counter that is used to set the counter state, such as UP/DOWN
d) The maximum number of states in a counter sequence
View Answer
Answer: d
Explanation: Modulus is defined as the maximum number of stages/states a counter has. It is independent of the number of states the counter will actually traverse.

143. A sequential circuit design is used to _____
a) Count up
b) Count down
c) Decode an end count
d) Count in a random order
View Answer
Answer: d
Explanation: A sequential circuit design is used to count in a random manner which is faster than the combinational circuit. It is used for storing data.

144. In general, when using a scope to troubleshoot digital systems, the instrument should be triggered by _____
a) The A channel or channel 1
b) The vertical input mode, when using more than one channel
c) The system clock

d) Line sync, in order to observe troublesome power line glitches
View Answer
Answer: c
Explanation: All the information is sent from one end to another end through the clock pulse which behaves like a carrier. So, for troubleshooting it should be triggered by the same. Since the system clock is internally produced.

145. Which counters are often used whenever pulses are to be counted and the results displayed in decimal?
a) Synchronous
b) Bean
c) Decade
d) BCD
View Answer
Answer: d
Explanation: BCD means Binary Coded Decimal, which means that decimal numbers coded of binary numbers. It displays the decimal equivalent of corresponding binary numbers.

146. The _____ counter in the Altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.
a) 74134
b) LPM
c) Synchronous
d) AHDL
View Answer
Answer: b
Explanation: The library of parameterized modules (LPM) counter in the Altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.

147. The minimum number of flip-flops that can be used to construct a modulus-5 counter is _____
a) 3
b) 8
c) 5
d) 10
View Answer
Answer: a
Explanation: The minimum number of flip-flops used in a counter is given by: $2^{(n-1)}<=N<=2^n$.
Thus, for modulus-5 counter: $2^2 <= N <= 2^3$, where N = 5 and n = 3.

148. The duty cycle of the most significant bit from a 4-bit (0–9) BCD counter is _____
a) 20%
b) 50%
c) 10%
d) 80%
View Answer
Answer: a
Explanation: There are 10 states, out of which MSB is high only for (1000, 1001) 2 times. Hence duty cycle is 2/10*100 = 20%. Since the duty cycle is the ratio of on-time to the total time.

149. Normally, the synchronous counter is designed using _____
a) S-R flip-flops
b) J-K flip-flops
c) D flip-flops
d) T flip-flops
View Answer
Answer: b
Explanation: Since J-K flip-flops have options of recovery from toggle condition and by using less number of J-K flip-flops a synchronous counter can be designed. So, it is more preferred. Also, because JK-flip-flops resolves the problem of Forbidden States.

150. MOD-16 counter requires _____ no. of states.
a) 8
b) 4
c) 16
d) 32
View Answer
Answer: c
Explanation: $2^n >= N >= 2^{(n-1)}$, by using this formula we get the value of N=16 for n=4.

151. What is a state diagram?
a) It provides the graphical representation of states
b) It provides exactly the same information as the state table
c) It is same as the truth table
d) It is similar to the characteristic equation
View Answer
Answer: b
Explanation: The state diagram provides exactly the same information as the state table and is obtained directly from the state table.

152. High speed counter is _____
a) Ring counter
b) Ripple counter
c) Synchronous counter
d) Asynchronous counter
View Answer
Answer: c
Explanation: Synchronous counter doesn't have propagation delay. Propagation delay refers to the amount of time taken in producing the output when the input is altered.

153. Program counter in a digital computer _____
a) Counts the number of programs run in the machine
b) Counts the number of times a subroutine
c) Counts the number of time the loops are executed
d) Points the memory address of the current or the next instruction
View Answer
Answer: d
Explanation: Program counter in a digital computer points the memory address of the current or the next instruction which is to be executed.

154. Fundamental mode is another name for _____
a) Level operation
b) Pulse operation
c) Clock operation
d) Edge operation
View Answer
Answer: b

156. Modulus refers to _____
a) A method used to fabricate decade counter units
b) The modulus of elasticity, or the ability of a circuit to be stretched from one mode to another
c) An input on a counter that is used to set the counter state, such as UP/DOWN
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