Microprocessor And Microcontrollers (MPMC)

Branch - ETC (Module - III, V)

Semester - 5th

Short Questions

2-Marks :-

Q.1) Name all the segment registers in 8086.

Ans→ The segment registers are :—

(i) CS → Code segment register
(ii) SS → Stack segment register
(iii) DS → Data segment register
(iv) ES → Extra segment register.

2) Why the ~~segm~~ memory segments limited to 64K in 8086 ?

Ans→ (i) As the registers present inside 8086 are capable of holding a maximum of 16 bit operand hence during any memory operations this registers cannot be used to hold the memory address efficiently.

(ii) Also, the instruction set is designed which doesnot support 20 bit address operand.

Hence, to avoid these problems the physical memory (1M) is divided into small memory blocks called as memory segments of 2^{16} = 64K capacity.

3) Why DMA mode of data transfer scheme is the fastest than normal data transfer ?

Ans→ In normal data transfer schemes, a data coming from I/O is first taken to Accumulator of the CPU and then stored in memory.

→ But in DMA scheme, data exchange takes place between memory and I/O, by passing the accumulator of CPU.

→ Since accumulator of CPU doesnot take part in DMA mode of data transfer scheme, thus this mode is fastest.

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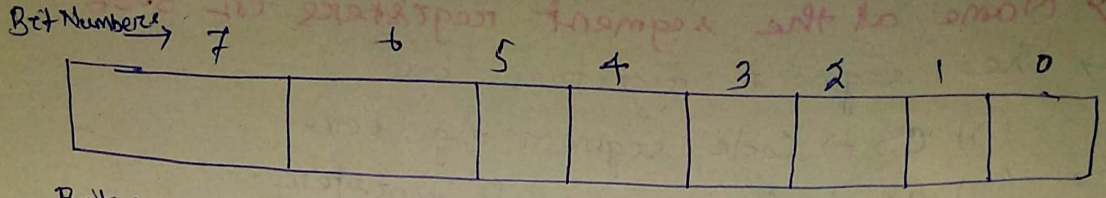
4) Explain the status register and its bit pattern of 8237 DMA controler.

Ans → The status register of 8237 DMA controller that contains information about the operating state of its 4 channels.



Bit 0 → channel 0 has reached TC
Bit 1 → channel 1 has reached TC
Bit 2 → channel 2 has reached TC
Bit 3 → channel 3 has reached TC
Bit 4 → channel 0 has request.
Bit 5 → channel 1 has request
Bit 6 → channel 2 has request
Bit 7 → channel 3 has request.

5) What is the function of ESP in 80386 µp?

Ans → ESP is the extended stack pointer which is of 32 bit.

→ It is used by the stack, call and return instructions.
→ It can be used as 16 bit stack pointer.
→ It is used to access information in stack segment of memory.
→ SP is the offset from the current value of the stack segment base address and select a specific storage location in the 64K byte stack segment.

6) What are the differences between the logical addresses and physical addresses?

Ans → Logical address :- Real mode architecture described by a segment base address and an offset where segment base address (CS, DS, ES, SS) are 16 bit and offset (IP, SI, DI, BX, DX, SP, BP) are 16 bit.

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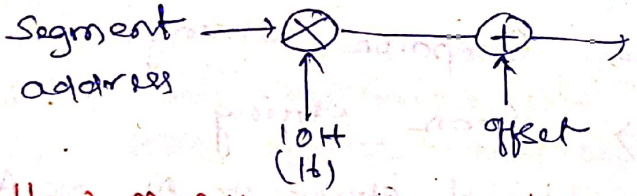
Ex:- CS:IP → 1050H : 1000H → code area

physical address :-

→ It is the actual address used for accessing memory of 20 bits in length.

→ It is formed by shifting the value of the 16 bit segment base address left 4 bit positions.



7) How many types of data communication is possible in 8251 USART?

Ans → As 8251 is universal synchronous, Asynchronous, receiver and transmitter; therefore communication can take place with 4 different ways i.e.

(a) Asynchronous transmission
(b) Asynchronous reception
(c) Synchronous transmission
(d) Synchronous reception.

8) Form control word for the following configuration of the ports of intel 8255 for mode 0 operation.

Port A = output, port B = output
Port C_{lower} = output, port C_{upper} = Input.

Ans → The control word bit for the configuration of the ports are

7	6	5	4	3	2	1	0	← Bit No
1	0	0	0	1	0	0	0	control Bits

8 8

The control word is 88_H.

9) How many interrupt levels can be handled by 8259?

Ans → A single 8259 can handle upto 8 levels of interrupts

→ Several 8259's can be cascaded to handle upto 64 levels of interrupts.

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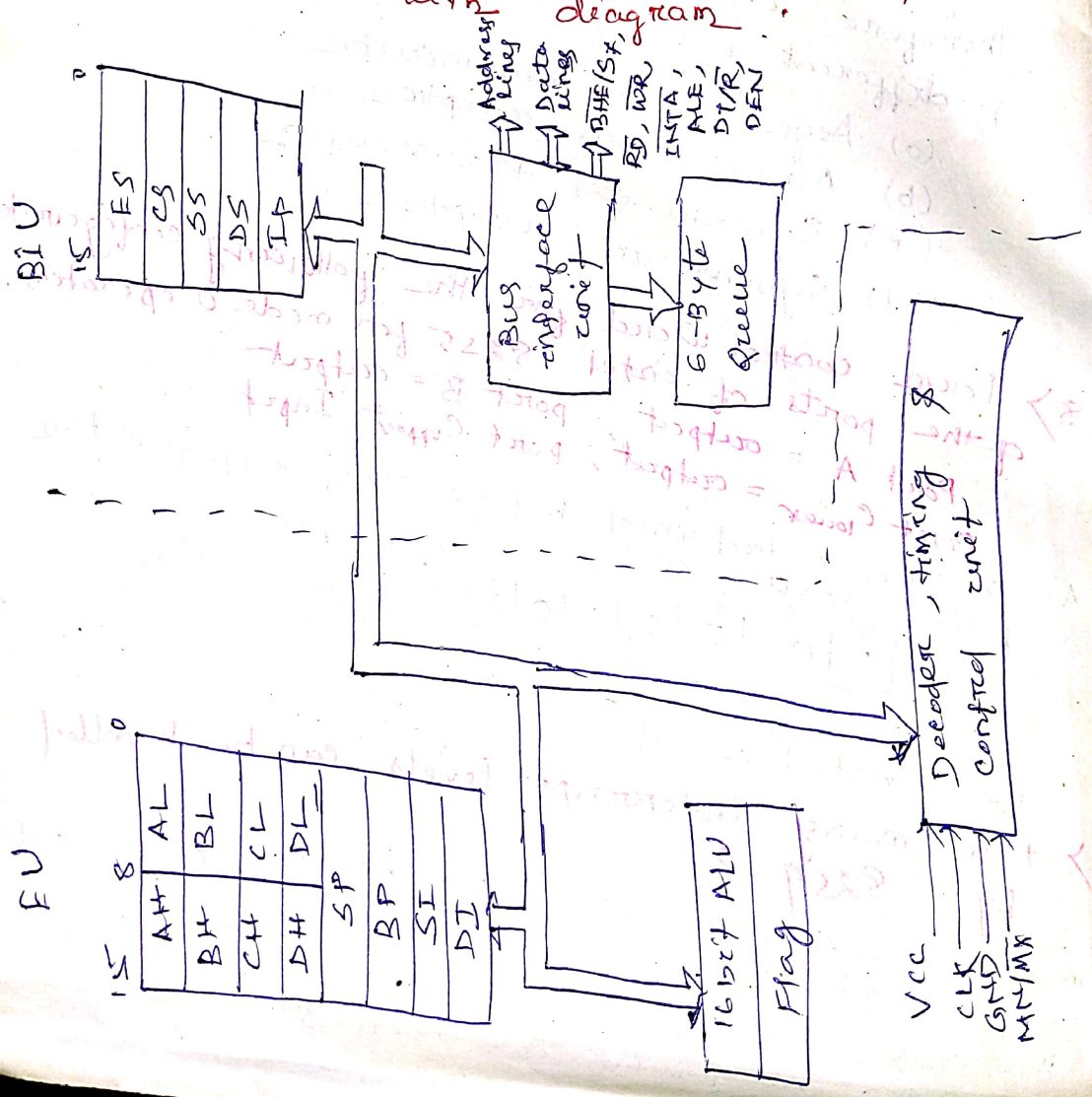
10) List the basic string instructions.

Ans) The basic string instructions are :-

Mnemonic	Operation
MOVS	Move byte or word string i.e. move string.
MOVSB	Move string byte
MOVSW	Move string word
CMPS	Compare string
SCAS	Scan string
LODS	Load string to AL or AX
STOS	Store string from AL or AX

Long Questions :-

Q.1) Explain the overview of 8086 internal architecture with diagram.



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→ functional block diagram of 8086 is divided into 2 functional units.
① BIU (Bus interface unit)
② EU (Execution unit)

EU:- The general purpose registers (GPRs), (SP) stack pointer, base pointer (BP), index registers (SI, DI), 16 bit ALU, flag along with decoder and timing & control unit ~~comb~~ combinely known as the execution unit.
→ this unit is responsible for decoding & execution of the instructions which are present in the 6 byte queue.

BIU:- All the segment registers and instruction pointer along with 6 byte queue are associated with bus interface unit.
→ The BIU handles transfer of data and address between processor and memory or I/O devices.
→ It also calculates the physical address of the instructions, fetches instructions from the address and stores them in the 6 byte queue which is to be executed further by EU.
→ whenever BIU is fetching any instruction from memory at the same time EU is taking the instructions from the queue which are already fetched by BIU.
→ Hence, both the functional units are operating on two different instructions providing less time for execution.
→ This type of overlapping operation of two functional units of 8086 µp is known as pipelining.

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2). Describe the function of following maximum mode pins of 8086 µP.
(i) QS_1, QS_0 (ii) $\bar{S}_2, \bar{S}_1, \bar{S}_0$ (iii) $\overline{LOCK}$

Ans- QS_1, QS_0 output :- These are the queue status signal. This status indicates the activity in the queue during the previous clock cycle i.e.

QS_1	QS_0	Status
0	0	No operation (queue is idle)
0	1	First byte of an opcode.
1	0	Queue is empty
1	1	Subsequent byte of an opcode

$\bar{S}_2, \bar{S}_1, \bar{S}_0$ output :- These three status signals indicate the type of transfer to be taken place during the current bus cycle.

S_2	S_1	S_0	Machine cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Memory Read
1	1	0	Memory write
1	1	1	Inactive/ passive

$\overline{LOCK}$ output :- Low on this pin indicates that other system bus master are not to gain control of the system bus.

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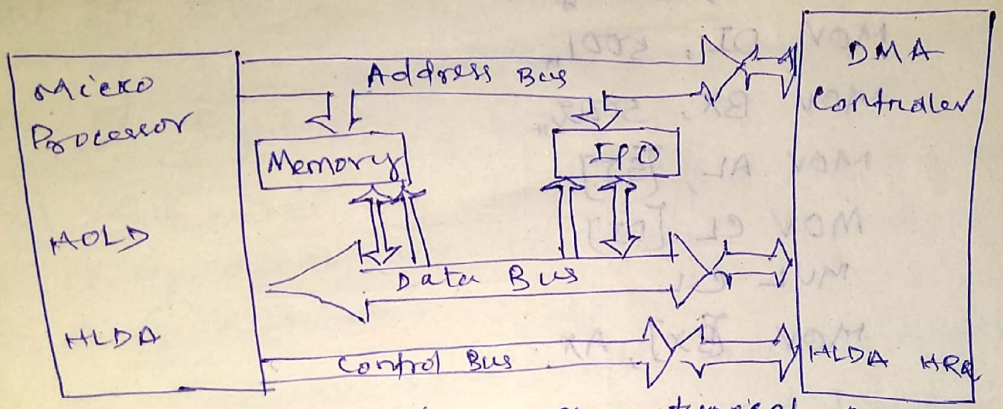
3) What is the purpose of DMA mode of data transfer? Provide a schematic diagram of DMA mode of data transfer.

Ans – Direct Memory access (DMA) is a technique that transfer data between a µp microcomputer's memory and I/O device without involving the µp.

→ DMA data transfer is divided into –
(i) Burst mode of DMA data transfer.
(ii) Cycle stealing technique of DMA data transfer.
(iii) Interleaved DMA.



→ The main function of a typical DMA controller are –
the I/O devices request DMA operation via the DMA request line of the controller chip. the controller chip activates the µp Hold pin, requesting the CPU to release the bus.

→ the processor sends $\overline{HLDA}$ back to the DMA controller, indicating that the bus is disabled.

→ the DMA places the current value of its internal registers on the system bus and sends a DMA acknowledge to the peripheral device the DMA controller completes the DMA transfer.

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4) Write an assembly language program for 8086 µp to multiply two 8-bit numbers stored in two different locations using both direct & indirect addressing.

Ans → Direct Addressing mode :—

```
MOV AL, [5000H]
MOV BH, [5001H]
MUL BH
MOV [5002H], AX
```

Using Indirect addressing mode :—

```
MOV SI, 5000H
MOV DI, 5001H
MOV BX, 5002H
MOV AL, [SI]
MOV CL, [DI]
MUL CL
MOV [BX], AX.
```

5) Describe about keyboard / Display controller 8279.

Ans → The features of 8279 are :—

(i) 8259 provides a scanned interface to a 64 contact key matrix with two more keys CONTROL and SHIFT.

(ii) 8279 provides 3 input modes for keyboard interface —
   a) Scanned keyboard Mode
   b) Scanned Sensor matrix mode
   c) Strobed input mode.

(iii) It has built in hardware to provide key debounce.

(iv) The interrupt output of 8279 can be used to tell CPU that the keypress is detected. This eliminates the need of software polling.

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→ (v) It provides 8 byte FIFO RAM to store keycodes. This allows to store 8 keyboard inputs when CPU is busy for an computation.

(vi) It provides multiplexed display interface with blanking and inhibit options.

(vii) It provides 16 byte display RAM to store display codes for 16 digits, allowing to interface 16 digits.

(viii) It has 2 o/p modes for display interface
a) Left Entry (type writer type)
b) Right Entry (Calculator type)

(ix) Simultaneous keyboard & display operation facility allows to interleave keyboard & display software.

(x) In autoincrement mode, address of display RAM & FIFO RAM is incremented automatically.

6) Explain the BSR mode of 8255.

Ans → BSR mode (Bit Set Reset) :—

→ In BSR mode port-C can operate in which can be set or reset by writing an appropriate control word in the control register.

→ A control word with D7=0 is recognised as a BSR mode control word.

→ The I/O operations of port A & B are not affected by the BSR control word.

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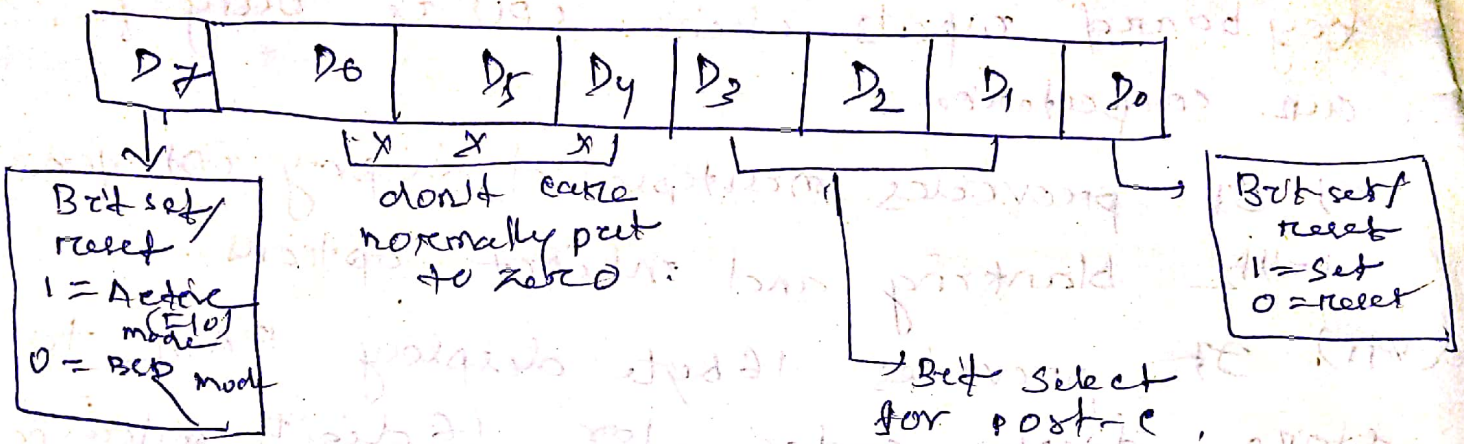
→ The control word format in BSR mode is -



D_3	D_2	D_1	Particular bit of Port C selected
0	0	0	Bit 0 PC_0
0	0	1	Bit 1 PC_1
0	1	0	Bit 2 PC_2
0	1	1	Bit 3 PC_3
1	0	0	Bit 4 PC_4
1	0	1	Bit 5 PC_5
1	1	0	Bit 6 PC_6
1	1	1	Bit 7 PC_7

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